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A new π/3-BPSK Digital Demodulator and Estimation of its Performance in UHF Transionospheric link

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Abstract - *This work shows a new architecture for π/3-BPSK demodulator intended to be part of a regenerative transponder (which will be on board nanosatellites), and operate in transionospheric links in the UHF band (~401 MHz). Also presented are the results of experiments, which show that the new architecture meets the specifications of the design of the system. The results of the experiments also show that the new architecture of the π/3-BPSK demodulator is more robust to the effects of ionospheric scintillation when compared to the version published in a previous work. To estimate the performance of the new proposed π/3-BPSK demodulator, experiments were made in the form of simulations to measure bit error rate take account offset, and carrier acquisition time with phase step. To compare the previous version of the demodulator to this new one, experiments were made in similar conditions but also in more severe conditions than those in which the previous version was tested. According to the experiments, the new version of the π/3-BPSK demodulator meets the specifications required in the transponder project when operating in an AWGN channel and there is reduction of cycle slips events when taking into account the effects of ionospheric scintillation than one developed in a previous work.*

Key Words: Transionospheric channel, ionospheric scintillation, performance of π/3-BPSK demodulator, regenerative transponder, communications through nanosatellites, PCDs, SBCDA, carrier recovery, transitory in synchronism, fluctuations of amplitude and phase on π/3-BPSK in UHF-band.

1. INTRODUCTION

To increase and modernize the Brazilian Environmental Data Collection System ("Sistema Brasileiro de Coleta de Dados Ambientais - SBCDA") using Data Collection Terminals-DCTs and satellites [1-3], the National Institute for Space Research ("INPE') is developing new regenerative transponders to be put on board nanosatellites [3].

The communications link between the sensors signal of DCTs ("PCDs - Plataforma de Coleta de Dados") and the transponder on the satellite operates in band UHF (~401 MHz) using π/3-BPSK modulation. The π/3-BPSK modulation is a variant of Binary Phase Shift Keying (BPSK) with modulation index π/3 in which the carrier is not suppressed [2], [3]. The signal with modulation π/3-BPSK contains a spectral line at the frequency of the carrier as shown on the spectrum of the Figure 4.17 in [4].

The band UHF in the SBCDA is used in hundreds of the environmental Data Collection Terminals for communication links to satellites SCD1 (NORAD ID 22409), SCD2 (NORAD ID 25504) and CBERS (NORAD ID: 40336). However, the literature [5-10] on the subject shows the space links below C-band can be severely affected by distortions caused by ionospheric scintillations typically present in the transionospheric links. Therefore, the previous work [8] motivated the authors to do this work.

In the previous version of the π/3-BPSK demodulator, presented in [3], the results of the computational simulations taking into account a transionospheric channel [8] showed that the previous solution from [3] presented multiple cycle slips events, even for the interval 5 dB ≤ E_b/N_0 ≤ 8 dB in S_4=0.2, and for 5dB ≤ E_b/N_0≤ 9dB and S_4=0.3 [8]. Therefore, this work proposes a new architecture for π/3-BPSK demodulator more robust to the effects of ionospheric scintillation than the one presented in [3].

The main contributions of this work are the design and evaluation of a simple non-squaring DPLL for π/3-BPSK demodulation, aiming to reduce hardware requirements and a more robust π/3-BPSK receiver taking into account the effects of cycle slips events when operating with ionospheric scintillations, as compared to the previous version presented in [3]. Therefore, the authors hope the new receiver architecture for π/3-BPSK demodulation will increase the QoS of the SBCDA and improve the DCTs localization service using satellites [11], [12].

This work is organized as follows: in Section II is described the scenery of π/3-BPSK links supposing an AWGN channel, induction of scintillation and the details of the subsystems that compose the demodulator. In Section III are shown the results of the evaluation of performance using computer simulations including some discussions. In section IV are presented the conclusions of this work and future perspectives.

2. DESCRIPTION OF THE SYSTEM AND ANALISYS

To explore the I/Q signal space containing various intensities of scintillation as occurs in the ionosphere and study the impact of the scintillation events on the performance of the future transponder based on π/3-BPSK

modulation [2-4], the authors describe in the following the simulation system used in this work. Assuming initially AWGN channel, the signal at the input of the demodulator is [3]:

$$r[n] = \frac{\sqrt{3}A}{2} b[n] \cos(\omega_c n + \theta_c[n]) + \frac{A}{2} \sin(\omega_c n + \theta_c[n]) + w[n], \quad (1)$$

where A is the amplitude of the received signal, ω_c is the discrete frequency of the carrier, $b[n]$ is the signal in baseband, $\theta_c[n]$ is the phase of the carrier and $w[n]$ is the noise AWGN with variance N_w [3].

The signals received by the satellite have duration between 360 to 920ms, beginning with a pilot signal lasting for 160ms without modulation. This initial interval of time is reserved for frequency and phase synchronization. The next 37.5ms of the message are the first 15 bits "1" used for symbol synchronization [3].

2.1 ARCHITECTURE OF THE NEW DEMODULATOR

The functional block diagram of the π/3-BPSK demodulator is presented in Figure 1.

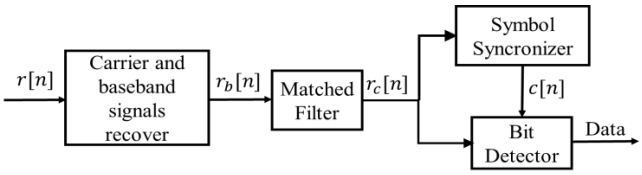

Fig. 1. Block diagram of the new π/3-BPSK demodulator.

The carrier recovery subsystem also generates the baseband signal $r_b[n]$, Equation (4), by mixing signal $r[n]$ with the recovered carrier $s[n]$, as can be seen in Fig. 2. However, in the second term $r_b[n]$ there is a component with $2\omega_c$. This component is filtered in the next stages composed of a matched filter [3], the symbol synchronizer and bit detector blocks, as seen in Fig. 1 and Fig. 3.

The symbol synchronizer and bit detector subsystem maximize the signal-to-noise relation, using a matched filter on signal $r_b[n]$. The impulse response of the matched filter is a discrete pulse, exactly as defined by Equation (3) in [3]. This filter maximizes the signal-to-noise ratio and eliminates the signals around $2\omega c$ present in signal $r_b[n]$.

Therefore, as explained in [3], the symbol synchronizer receives $r_c[n]$ from the matched filter [3] and generates a square wave, denoted $c[n]$, which is synchronized to the beginning and end of the symbols thus represents the system *clock.* Details of a synchronizer similar to the one used in this work can be seen in [3].

The signals $r_c[n]$ and $c[n]$ are delivered to the bit detector subsystem, Fig. 3, which, from these signals, detects the bits and delivers the data sequence recovered by the π/3-BPSK demodulator, as seen in the block diagram of the system shown in Fig. 1, and in more details in Fig. 3.

2.2 CARRIER RECOVERY AND BASEBAND SIGNAL

The architecture of the carrier recovery system in this work is different from that one presented in [3]. We choose a nonsquaring DPLL architecture, as described in Fig. 2, because the carrier signal is present all the time on π/3-BPSK modulation, as shown by Equation (1), and in general, for a nonsquaring loop, the cycle slip jump equal to 2π has not any significant effect in carrier synchronization [13]. Therefore, taking into account the effects when operating with ionospheric scintillations, the new architecture can reduce loss of lock as compared to the previous version presented in [3].

To use the symbol synchronizer and the bit detector similar those presented in previous version [3], the signal $s[n]$ generated by the NCO needs represent the recovered carrier $\cos(\omega_c n + \hat{\theta}_c[n])$, similar to the signal $s[n]$ presented in [3]. However in this new version of demodulator $s[n]$ is obtained using the NCO of Figure 2, built as follows.

$$s[n] = \cos(\omega_c n)\cos(\hat{\theta}_c[n]) - \sin(\omega_c n)\sin(\hat{\theta}_c[n]), \quad (2)$$

where $\hat{\theta}_c[n] = G_{NCO} \sum_{i=\infty}^{n-1} s_{LF}[i]$, and s_{LF} is the signal exiting the Loop Filter in Figure 2.

Using trigonometry $\cos(\alpha + \beta)$, $s[n]$ can be written as:

$$s[n] = \cos(\omega_c n + \hat{\theta}_c[n]), \quad (3)$$

where $\hat{\theta}_c[n]$ represents the estimative of carrier phase.

To calculate the recovered phase, the noise represented by $w[n]$, in Equation (1), was considered negligible. Therefore $s[n]$ is the recovered carrier, compatible with the symbol synchronizer and bit detector shown in Figure 3, similar to the symbol synchronizer and bit detector developed and presented in [3].

However, different from [3], apart from the recovery of the signal of the carrier, one can note that the baseband signal $r_b[n]$ is generated by the mixer at the entry in Figure 2, resulting from the product of signal $r[n]$ with signal $s[n]$ generated by the NCO. Therefore $r_b[n]$ is obtained as follows:

$$r_b[n] = \frac{\sqrt{3}A}{4} b[n] + \frac{\sqrt{3}A}{4} b[n]\cos(2\omega_c n + 2\theta_c[n]) - \frac{A}{4}\text{sen}(2\omega_c n + 2\theta_c[n]) + w[n]\cos(\omega_c n + \theta_c[n]). \quad (4)$$

In Equation (4) one can note that the first term represents the baseband signal containing the transmitted information.

To define the Loop Filter, the discrete-time loop represented in Figure 2 was approximated by a second-order linear system [14], [15] whose system function:

$$H(z) = \frac{\hat{\theta}_c[z]}{\theta_c[z]} = \frac{(g_1 + g_2)z - g_1}{z^2 - (g_1 + g_2 - 2)z + (1 - g_1)}, \quad (5)$$

where g_1 and g_2 are the gains of the loop filter, respectively the gain of the proportional part and the gain of the integrator, similar to a PI loop (Proportional+Integral loop), with natural frequency ω_n and dumping rate ζ. This loop is inspired by an analogical loop PI, however the model is for a discrete-time loop [14], as presented in following Figure 2:

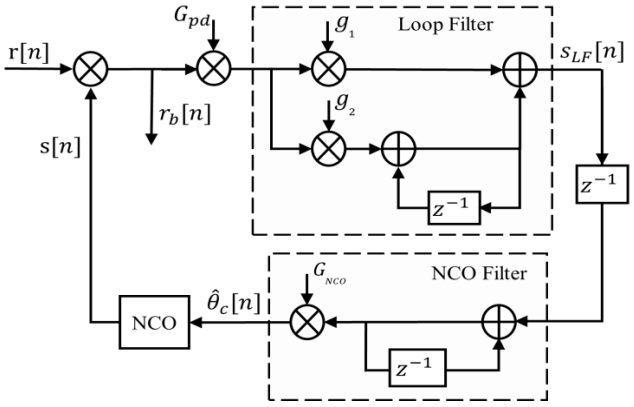

Fig. 2. Block diagram of the DPLL.

Due to the specifications of the design, presented in [3], the maximum acquisition time for the carrier must be $t_{max} = 160ms$, therefore the authors used as steady-state time $t_s = 140$ms for $\zeta = 0{,}707$, and used the following approximation [14], [16]:

$$t_s \cong \frac{4}{\omega_n \zeta}, \quad (6)$$

obtaining $\omega_n = 40{,}41$.

To simplify calculations the value adjusted for input gain was $G_{pd} = 3.83$. The gains g_1 and g_2 are given from the following equations [14]:

$$g_1 = 1 - e^{2\zeta w_n T_s} \quad (7)$$

$$g_2 = 1 + e^{2\zeta w_n T_s} - e^{2\zeta w_n T_s} \cos\left(w_n T_s \sqrt{1 - \zeta^2}\right), \quad (8)$$

which results in $g_1 = 1.4283\text{x}10^{-4}$ and $g_2 = 4{,}0822\text{x}10^{-8}$.

Therefore the function of the PLL presented in Figure 2 is to estimate the phase of the carrier $\hat{\theta}_c[n]$, generate the baseband signal $r_b[n]$ and eventually some frequency *offset*.

In this model of simulation the value adjusted for G_{pd}, and the values obtained for g_1 and g_2, did not require any adjustment in G_{NCO}. Therefore in this configuration the authors used G_{NCO}=1. Eventually, in the final discrete-time version in hardware the mixer at the output of the NCO filter, mixer with gain G_{NCO}= 1, may be suppressed.

2.3 SYMBOL SYNCRONIZER AND BIT DETECTOR

The symbol synchronizer and the bit detector were adapted from the demodulator presented in [3]. However, this new configuration excludes the mixer at the input of the symbol synchronizer in block diagram presented in [3]. Noting that the signal $r_b[n]$, at the input of the matched filter is already generated by the mixer at the entry of the DPLL, as can be seen in Fig. 2. In a simplified form, these subsystems are summarized in Fig. 3. The solution the authors used is a version of the quadratic synchronizer [17-19], very similar to that presented in [3].

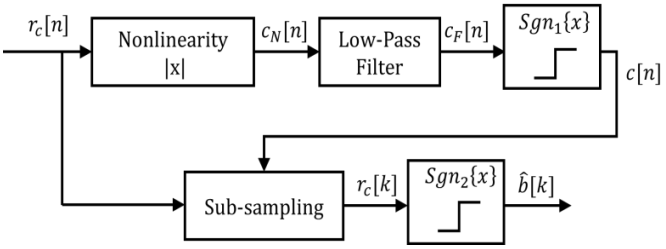

Fig. 3. Block diagram of the symbol synchronizer and bit detector adapted from [3].

In this architecture for symbol synchronizer, because of the high oversampling rate (N_T >> 1), it is not necessary to use interpolators to determine the best sample for decision, as shown in [3].

The block diagram in Fig. 3 also shows the bit detector subsystem. However, the input signal $r_c[n]$ is generated from the matched filter presented in Figure 1. That subsystem is similar to the symbol synchronizer and bit detector blocks presented in [3]. The signal $r_c[n]$ goes through a subsampler which chooses a sample per symbol, controlled by the raise of the *clock* $c[n]$, to generate the signal $r_c[k]$. Meanwhile the limiter receives the signal $r_c[k]$ and defines the output $\hat{b}[k]$ as detailed em [3].

It should be highlighted that the raise of $c[n]$ indicates the beginning and the end of each symbol. The decision about the bit received is made by the limiter $Sgn\{x\}$. $Sgn\{x\}$ is equal to 1 if $x \geq 0$ and is equal to -1 if $x < 0$. The bit $\hat{b}[k]$ estimated will represent "1" when $r_c[k]$ is bigger or equal to zero, and will be "0" when $r_c[k]$ is smaller than zero.

Next is presented a summary of the performance of the proposed π/3-BPSK demodulator, in terms of variation of the estimated phase using the Cramér-Rao criteria [19], carrier acquisition time and bit error rate. The experiments were made using the simulation system presented in [8], configured to evaluate the requirements of the design as presented in [3], and as suggested in [8]. In Section III, the authors also show the results of the

performance of this new version when submitted to the effects of scintillation

3. RESULTS AND DISCUSSION

In this section are shown main results of the performance of the proposed π/3-BPSK demodulator, obtained using computational simulation. Aiming to meet the project specifications, in this work were evaluated the Cramér-Rao limit, acquisition time for synchronism of the carrier and bit error rate in an AWGN channel. Besides these were evaluated also the bit error rate taking into account diverse intensities of S_4.

The values of the main parameters used in the model and simulations are summarized below in Tab. 1:

Table -1: Parameters of the project specifications from [3]

• Carrier frequency: $f_c = 50$ kHz;
• Symbol tax: $1/T = 400$ bps;
• Sampling frequency: $F_s = 200$ kHz ;
• Bit energy per noise density: 5 dB $\leq E_b/N_0 \leq$ 30 dB;
• Carrier acquisition time $\leq$ 160 ms
• Operating frequency 401 MHz
• Phase offset: 0 to 2π
• Subcarrier frequency offset: $\pm$5 Hz
• Synchronization time: 37.5ms

3.1 VARIANCE OF THE ESTIMATED PHASE

To evaluate the robustness of the phase estimator of the proposed demodulator, taking into account the design specifications from [3] presented in Tab. I, the authors made communication link simulations in the interval 5dB $\leq E_b/N_0 \leq$ 30dB, as presented in Fig. 4.

In these experiments, the variance of the phase error was estimated by computational simulation. Therefore, the system of simulation was configured for AWGN channel with design parameters in Tab. I.

The values measured at the output of the NCO filter, Fig. 2, are compared to the theoretical Cramér-Rao bound, shown below [19]:

$$MCRB(\theta) = \frac{1}{2L_{eq}LE_b/N_0}, \quad (9)$$

$$L_{eq} = \frac{1}{2B_LT} \quad (10)$$

where $2B_L$ is the noise bandwidth [15].

Therefore, Figure 4 presents the curve of the Cramér-Rao limit (Equations 9 and 10) and the curve of the estimated variance. It can be noted that the measured variance approaches the Cramér-Rao bounder when $E_b/N_0 > 15$dB.

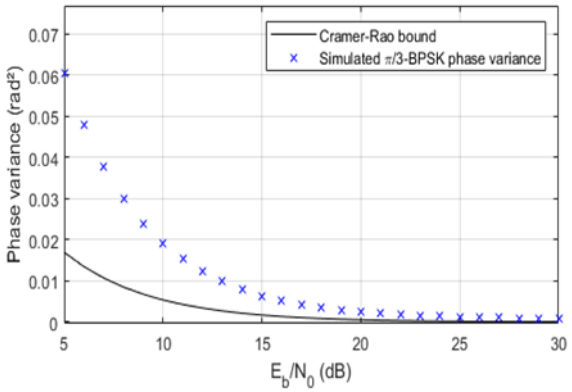

Fig. 4. Variance of the estimated phase.

3.2 CARRIER ACQUISITION TIME

To evaluation of the phase deviation during the carrier acquisition, Fig. 5 shows the transitory of the loop phase of the DPLL changed to a step of $\pi/3$, E_b/N_0=30 dB.

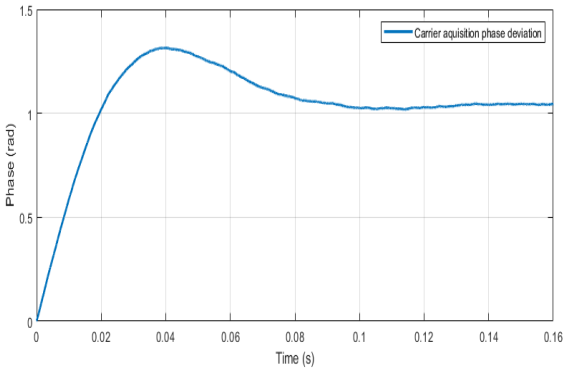

Fig. 5. Transitory outputs of the loop for a phase step.

According to the tests, the steady-state time (t_s) is smaller than 140ms, so the design specification (Tab. 1) for acquisition of carrier in 160ms is met.

In the tests, not only the carrier acquisition occurred in less time than specified, examining the transitory at the output of the low-pass filter (of the symbol synchronizer) shown in Fig. 3, using the symbol synchronizer similar to that presented in [3], one can verify that stability is reached in less than 5 bits. Therefore, take in account the AWGN channel the synchronization occurs in time smaller than the specified 15 bits or 37.5ms.

3.3 BIT ERROR RATE

To estimate the bit error rate some curves of the BER of the demodulator are shown in Fig. 6. Curve 1 shows the theoretical performance of the BPSK modulation. Curve 2 is the null offset for frequency, phase and symbol delay. Finally, Curve 3 shows the BER of the demodulator with frequency offset equal to 30 Hz and symbol delay equal $T/2$. Even with 30 Hz offset one can note that the proposed demodulator has no significant loss compared to the output with no offset.

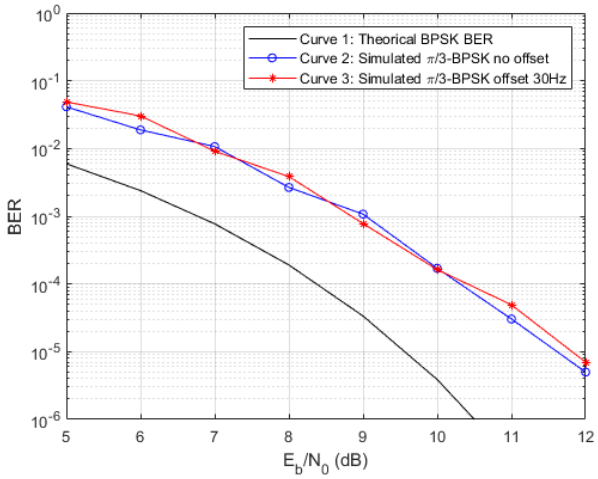

Fig. 6. Bit error rate curves of the demodulator in AWGN channel.

Therefore, if compared to previous version presented in [3], one expects a noticeable reduction in the resources needed to process the signals when implementing the system, because of the possibility of decreasing the resolution of the primary subsystem for estimation of the frequency, when detecting the signal of the PCD in the beginning of the link.

To evaluate the bit error rate when the demodulator operates with the variations of amplitude and phase similar to those found in the transionospheric channel, the authors made experiments taking into account the modification of the discrete time signal $r[n]$ at the input of the demodulator, as explained in details and presented in [8].

Therefore, all experiments were made in the simulation system used in [8], configured to simulate sceneries of on AWGN channel and links with diverse intensities of S_4. In what follows are shown, in Fig. 7, the results of BER for S_4=0.3, S_4=0.5 and $t \geq 60$s.

Apart from the tests to examine the robustness (through variance) of the estimated phase and experiments to examine the bit error rate in an AWGN, many other experiments were made taking into account also the influence of scintillation for $0.01 \leq S_4 \leq 1.0$ e $5\text{dB} \leq E_b/N_0 \leq 30\text{dB}$. In these tests for the interval $0.01 \leq S_4 \leq 0.4$ and $E_b/N_0 \geq 5$ dB there was no cycle slip, even taking into account a step of $\pi/3$.

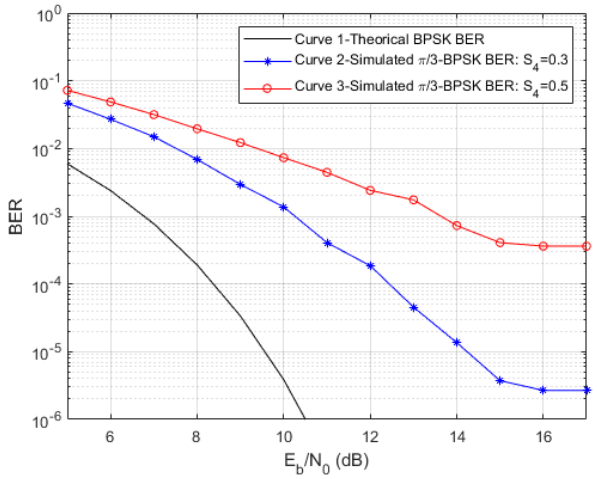

Fig. 7. Bit error rate curves taking into account some estimative of the effects of the transionospheric links.

During the experiments made to generate Fig. 7 for S_4=0.3 and S_4=0.5 in the interval $5\text{ dB} \leq E_b/N_0 \leq 17\text{ dB}$, the system did not show any cycle slip for S_4=0.3. However, for $S_4 \geq 0.5$ e $E_b/N_0 \leq 5$ dB cycle slips events may occur, and if one takes into account severe ionospheric scintillation, such as $S_4 > 0.7$, the system may have phase deviation.

4. CONCLUSIONS

This paper presents the design of a new coherent π/3-BPSK demodulator, with software defined architecture, to be used on the data collection satellites of SBCDA, as part of a new on-board regenerative transponder.

The paper presented the block diagrams and equations of the functional subsystems, and the details necessary for the mathematical analysis of the new architecture, to allow good use of the functionality of the symbol synchronizer and bit detector subsystems, similar to those developed in previous work [3].

However, taking into account that the blocks of the synchronizer presented in the earlier version are similar to this version, and noting that the phase recovered in this new version is a simplified version of the previous work, one can conclude that the new version requires much less digital processing resources than the previous one. This economy in hardware/software and consequent small energy demand is a factor extremely important when the objective is to build satellite transponders with a big number of simultaneous reception channels.

Beyond the evaluation of performance taking into account the AWGN channel this paper also presented tests and evaluations in diverse scenarios of links simulated under the effects of fluctuations in amplitude and phase, similar to the expected effects in links under ionospheric

scintillation when the satellite is in data reception from PCDs operation on land.

The results of the tests using computational simulation show that the solutions used for recovery of the carrier and the synchronism of symbol allow synchronization of the system in less time than that specified, beyond provoking little impact on the ratio E_b/N_0 in AWGN channel. In the operational situation for the AWGN channel when there is frequency *offset* and symbol delay the performance of the proposed demodulator in terms of BER is smaller than 2.5dB inferior to the theoretical limit in the condition BER = 10^{-4}.

However, as recommended in [8], [9], apart from the simulations to evaluate the performance of the new demodulator in AWGN channel, the authors did many others tests taking into account the effects of fluctuations in amplitude and phase expected for the transionospheric channel.

These additional tests, taking into account the effects of fluctuations in amplitude and phase, also were made to examine the performance of the demodulator in diverse link conditions. To this additional evaluation, the authors assumed transionospheric links as an AWGN channel added to several intensities of S_4 using computational simulations, similar to that presented in [8], according to the expected severity in diverse conditions of ionospheric scintillation and diverse intensities of the modulated signal in the receivers of the transponder.

The results of the computational simulation, taking into account the effects expected for the transionospheric channel, show the solutions used for recovery of the carrier and the symbol synchronism allow synchronization of the system in less than the 160ms imposed by the specifications of the project for AWGN channel and too in the interval $0.01 \leq S_4 < 0.5$ and $E_b/N_0 \geq 5$ dB. However, when taking into account the effects of scintillation one can verify increase in the BER as presented in Fig. 7. Besides, for $S_4 \geq 0.5$ and $E_b/N_0 \leq 5$ dB the system may present cycle slips events.

The paper showed new π/3-BPSK demodulator and an estimate of its performance to be part of a new transponder for data collection satellites, operating in UHF in the transionospheric channel. However, although the performance of this new demodulator has superseded the performance of the previous version [3], this work show the severity of the effects of ionospheric scintillation on space links will still demand new research aiming mitigate these effects on space communication devices, particularly significant to exchange data between ground and orbital segments below C-band [5-10].

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