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A VLSI Architecture of the Bilateral Filter for Real-Time Image Denoising

G.Premamai[1], G.Rajendra[2]

[1]P.G Student, Department of Electronics and Communication Engineering, Vkr,Vnb& Agk college of Engineering, Gudiwada, Andhra Pradesh,India
[2]Associate Professor, Department of Electronics and Communication Engineering, Vkr,Vnb&Agk college of Engineering,Gudiwada ,Andhra Pradesh,India

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Abstract *The Bilateral filter is a popular non-linear filter used for image denoising , edge detection, and texture analysis. However, it requires a large number of computations for each pixel, making it computationally intensive and challenging to implement in real time applications. A VLSI architecture of the Bilateral filter is to denoise a picture. The proposed architecture uses distance-oriented grouping, resource sharing,* and LUT techniques to reduce hardware complexity, power consumption, and computation time. The outcomes of the experiments demonstrate that the suggested architecture can carry out instantaneous picture denoising. with high accuracy and minimum hardware resources. The suggested design is expected to be useful for various real-time image-processing applications, including medical imaging, video surveillance, and autonomous driving.

***Key Words*: Bilateral filter, VLSI architecture, instantaneous picture Denoising, distance-oriented grouping, resource sharing, LUT.**

1.INTRODUCTION

A well-liked non-linear filter for image denoising, edge detection, and texture analysis is the bilateral filter. However, because it necessitates several computations for every pixel, it is computationally demanding and difficult to apply in real-time applications. To denoise pictures, a VLSI design of the bilateral filter is presented. Results show that the recommended design, resource sharing, and LUT approaches may decrease the complexity of the hardware, the amount of power used, and the amount of time it takes to compute. The results of the experiments show that the recommended architecture is capable of real-time picture denoising with high precision and little hardware overhead. The proposed architecture is anticipated to be beneficial for several real-time image-processing applications, including autonomous driving and medical imaging.

1.1 Motivation

Hardware designs that can execute complicated image processing algorithms have been developed in response to the growing need for real-time image-processing software. The computationally demanding approach known as the bilateral filter necessitates doing several computations for each pixel. In order to accomplish real-time picture denoising, a VLSI design of the bilateral filter is suggested in A VLSI design of the Bilateral Filter for Real-Time picture Denoising. To get over the computational complexity and power consumption restrictions of conventional solutions, which are frequently unsuitable for real-time applications, the bilateral filter was developed as a VLSI design for real-time picture denoising.

1.2 Problem Definition

The problem addressed in this Bilateral Filter VLSI Architecture for Real-Time Image Denoising is the high computational complexity and power consumption of the bilateral filter, which limits its use in real-time image processing applications. The Bilateral filter is a non-linear filter that requires a large number of computations to be performed for each pixel, which makes it computationally intensive on challenging to implement in real time applications. Additionally, the traditional software implementations of the Bilateral filter due to their incompatibility with hardware implementation high hardware complexity and power consumption.

2. Literature Survey

In the examination of the literature, several studies on We looked at the bilateral filter and its uses. Multiple techniques are utilized to implement the bilateral filter in hardware and software. Some of the major findings of the literature review are as follows: Popular non-linear filter for image processing is the bilateral filter. applications, such as image denoising, edge detection, and tone mapping.

a. Due to the many consumptions need for each pixel, the bilateral filter has a high computational cost making it computationally demanding and difficult to apply in real time applications.

b. Researchers have suggested a number of methods, such as distance-oriented grouping, resource sharing, and LUT approaches, to reduce the computational complexity and power consumption of the bilateral filter.

c. According to the literature study as a hole, the bilateral filter is a common filter for image processing applications, and there are numerous methodologies and implementations to optimizes its computationally complexity and power consumption.

d. The bilateral filer's suggested VLSI design from A VLSI of the bilateral filter for real time image using this discovery's as a foundation denoising offers a useful and effective method for real-time picture denoising reduce the amount of processing and energy used. Bilateral filter overview.

Geometric and photometric components make up the bilateral filter for grayscale and colour pictures. The spatial filter used to implement the geometric component, also known as the domain filter, is frequently defined as a low-pass filter. The domain filter can finish the full denoising procedure by averaging the values of neighboring pixels. However, while denoising, linear averaging excessively blurs the edges of objects. A range filter, a photometric component is employed to maintain the borders by averaging adjacent pixel values. The range filter is a nonlinear component that is programmed to ignore any pixel, regardless of location, whose value deviates from the value of the centre pixel in the filter window by a certain amount. The following sentences provide a description of the bilateral filter.

$$\hat{f}(x,y) = \frac{K(x,y)}{N(x,y)} = \frac{\sum_{(s,t)\in\Omega} f(x,y)\, W_d(s,t)\, W_r(s,t)}{N(x,y)}$$

When Gaussian noise is taken into consideration, the formulas (2) and (3), both of which are derived from the Gaussian curve, are used to describe Wd (s, t) and Wr (s, t) respectively:

$$W_d(s,t) = \exp\left(-\frac{D(f(x,y), f(s,t))^2}{2\sigma_d^2}\right),$$

$$W_r(s,t) = \exp\left(-\frac{\delta(f(x,y), f(s,t))^2}{2\sigma_r^2}\right),$$

where D(f (x, y), f (s, t)) and (f (x, y), f (s, t)) represent the Euclidean distance and intensity distinction between the current pixel f(x, y) and its neighbour pixel f(s, t), respectively, and d and r control the width of the Gaussian curve assigned to Wd (s, t) and Wr(s, t). The operation rule prevents the photometric component from being determined beforehand, necessitating the division in normalisation equation-3.

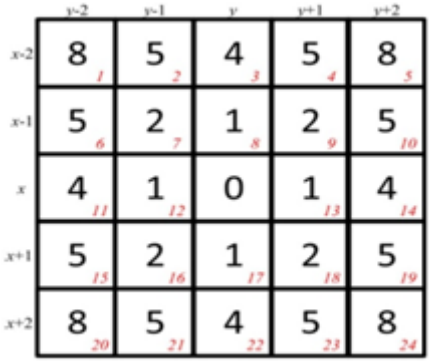

Fig -1: Arrangement focused on distance for windows 5 by 5in size.

In order to ensure that the range of the filter pictures does not exceed the defined limitations as a result of filtering, the normalization term is then carried out with N(s, t):

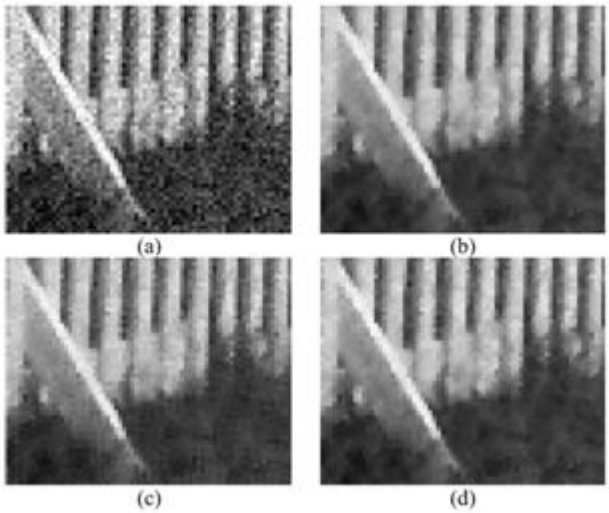

Fig -2: The following are the results for lighthouse notation (a) a noisy image with a standard division of 20; (b) filter using a software-oriented bilateral filter; (c) Filter using a fully synchronized design of a bilateral filer based on an FPGA for real-time denoising ; (d) filter using the suggested design.

$$N(x,y) = \sum_{(s,t)\in\Omega} W_d(s,t)\, W_r(s,t).$$

The Bilateral filter excels in the areas of edge recognition, texture removal, tone mapping, and picture denoising. Based on the idea of weighted average of nearby pixels, it is a sort of smoothing filter that maintains edges while reducing noise.

2.1 Existing systems

Noise-Aware and Light Weight VLSI Design of Bilateral Filter for robust and Fast Image Denoising for mobile system.

This system was proposed by Sung-Joon Jang and Youngbae Hwang in their research paper, "Noise-Aware and Light-Weight VLSI Design of Bilateral Filter for Robust and Fast Image Denoising in Mobile Systems." The paper also suggests a binary range kernel that reduces the complexity of the range kernel by substituting binary operations for range kernel operations. A noise-aware bilateral filter (NABF) based on the suggested binary range kernel is presented in Noise-Aware and Light-Weight VLSI Design of Bilateral Filter as a fully parallel and pipelined VLSI architecture. Field-programmable gate array (FPGA) implementation of the design proved successful.

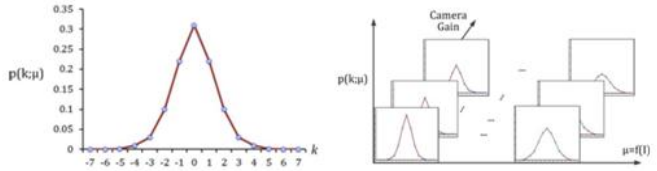

Fig-3 : Difference-based image noise and pixel intensity.

A small, noise-conscious bilateral filter Fast and Reliable Image Denoising in Mobile Systems Using VLSI Design The authors Sung-Joon Jang and Youngbae Hwang suggested this technology, called Noise-Aware and Light-Weight. According to a study titled "VLSI Design of Bilateral Filter for Robust and Fast Image Denoising in Mobile Systems," the range kernel may be made simpler by employing a binary range kernel, and noise can be estimated using a model for visual noise based. The proposed binary range kernel-based noise-aware bilateral filter (NABF) is described as a fully parallel and pipelined VLSI design in VLSI Design of Bilateral Filter.

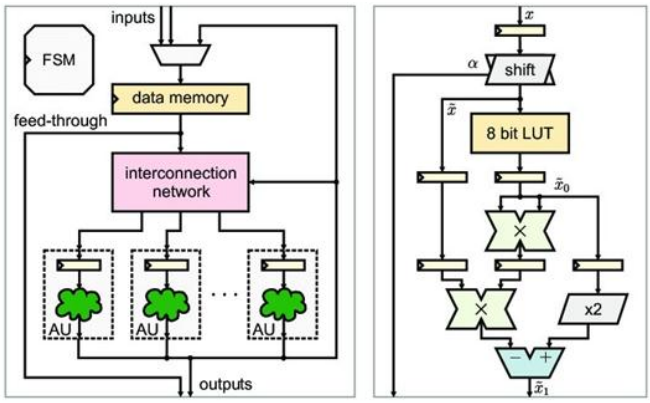

Fig-4: Bilateral filter with noise-awareness proposed VLSI architecture.

Here, the letters R stand for registers, ADD and SUB for adders and subtractors, MULT and DIV for multipliers and divisions, M and MUX for multiplexers, and ABS and COMP for comparison logic and absolute operations, respectively. The proposed binary noise-aware bilateral filter is implemented in a VLSI. an image window of 5 by 5 pixels is supported by a fully pipelined and parallelized hardware architecture for each clock.

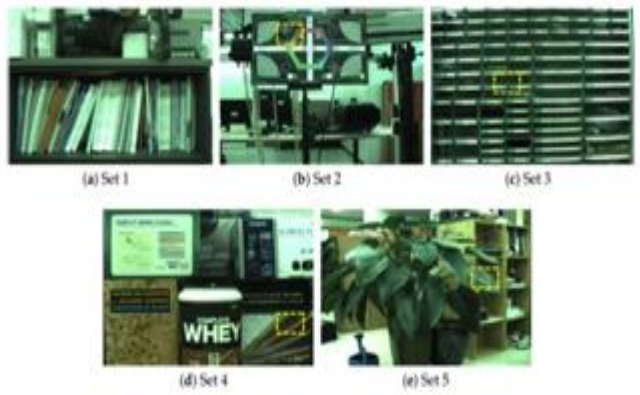

Fig-5: For the evaluation's data set. As evident For testing the suggested strategy, we took pictures of highly-textured and variously coloured settings from (a) to (e). The areas that will be expanded for the offered qualitative comparison are those with yellow dashed borders.

3. PROPOSED METHOD

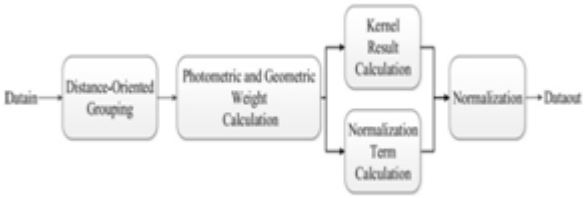

Fig-6: Suggested VLSI architecture block diagram.

The precomputed the values of Gaussian function, which are required for effective processing, are also stored in a memory module included in the suggested design. Real-time image-denoising applications can use the architecture since it has been optimized to lower hardware costs and speed up processing.

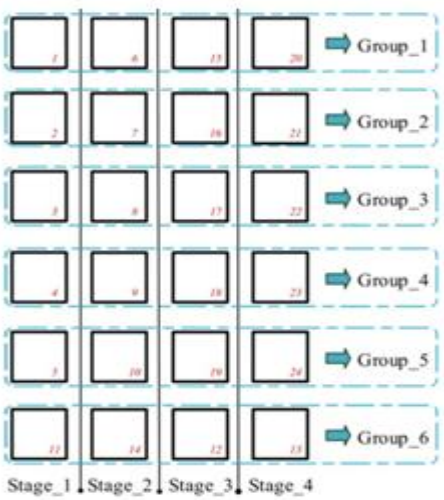

Fig-7: Position-oriented grouping of window size 5 × 5 from PPRM.

For real-time applications, bilateral filtering must be implemented on hardware. Several bilateral hardware designs have been developed and implemented using Field Programmable Gate Arrays (FPGAs). After grouping the input data, the recommended kernel-based method would process the whole 5 by 5 filter window in one pixel clock cycle. The Euclidean distances D(f (x, y), f (s, t)) between the current pixel at location (x, y) and its 24 neighbors are shown in Fig. 3in a 5 by 5 filter window.

4. SOFTWARE REQURIREMENTS

In addition to supporting programming languages like Java, C#, etc., it also has its own Integrated Development Environment (IDE) and library collection. Originally known as the matrix programming language, the acronym MATLAB stands for "Matrix Laboratory." It is a programming language of the fourth generation.

Fig-8: Matlab software.

Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of hardware description language (HDL) designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis. Vivado represents a ground-up rewrite and re-thinking of the entire design flow (compared to ISE). Like the later versions of ISE, Vivado includes the in-built logic simulator. Vivado also introduces high-level synthesis, with a toolchain that converts C code into programmable logic.

Fig-9: Xilinx vivado software.

5. RESULTS

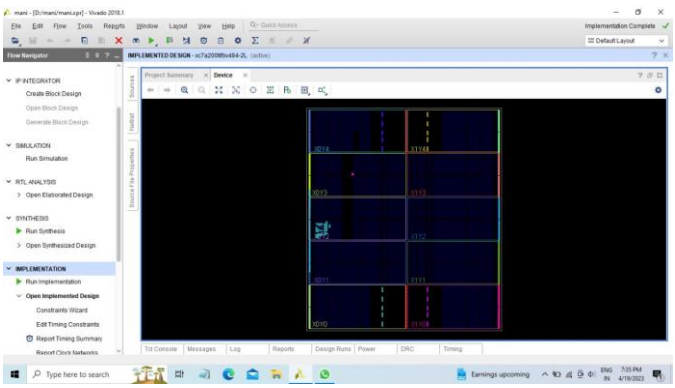

Fig-10: Sort 9 device.

The device was connected to Matlab through the Sort9 port. These stages include the input/output buffer, the grouping and sorting unit, the LUT unit, the distance calculation unit, the weight calculation unit, the normalization unit, the filter implementation unit, the memory unit, and the output unit.

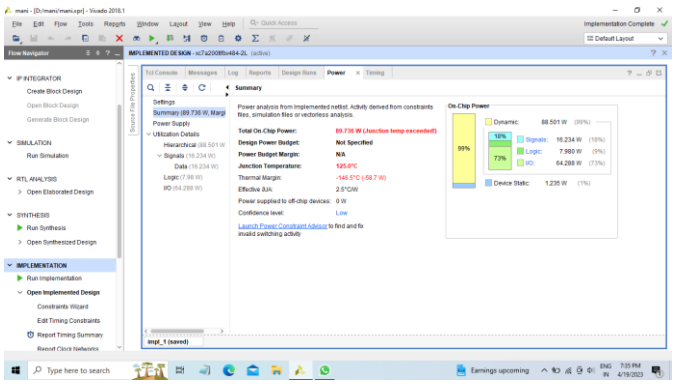

Fig-11: Power report for sort 9.

The power consumption report alludes to a study of the proposed VLSI architecture's power use. To simulate the power consumption of the design while taking into account numerous characteristics, such as clock frequency, supply voltage and transistor sizes.

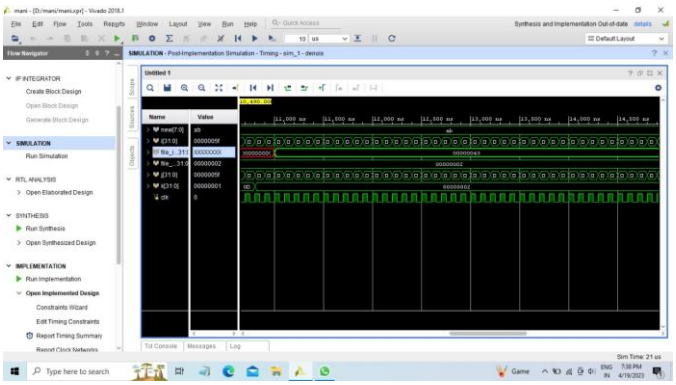

Fig-12: Sort 9 graph.

The set of nine graphs that are to evaluate how well the bilateral filter performed on the supplied input photos. The denoising outcomes are shown in these graphs. These graphs represent the denoising results obtained by the algorithm for different input images.

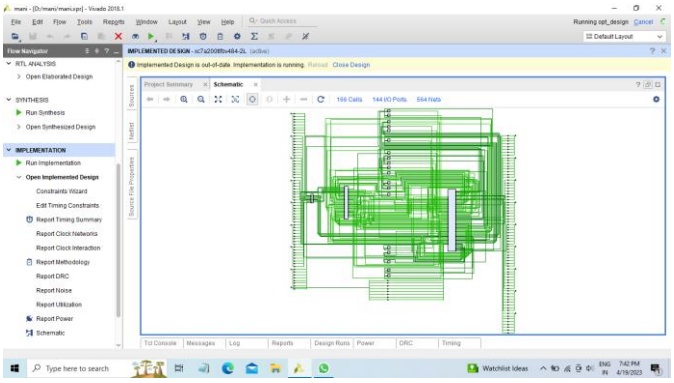

Fig-13: Sort 9 schematic.

The Sort 9 Schematics refer to the schematic diagrams of the 9 different stages of the bilateral filter architecture.

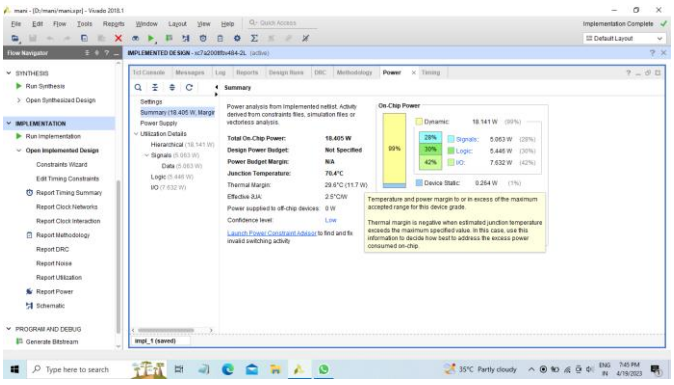

Fig-14: Power report for bilateral filter.

The power report details the total amount of power used by the circuit moreover, the amount of power used by each individual circuit component. This analysis is crucial because it aids in the circuit's power consumption optimization, which is a crucial factor in the design of affordable and energy-efficient systems. It enables the modification of the circuit's most power-hungry components.

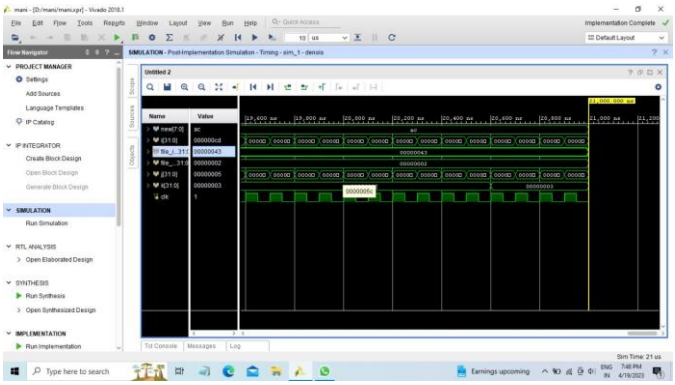

Fig-15: Midean graph.

The Midean Graph is a graph that shows the comparison of the filtering efficiency between the Median filter and the Bilateral filter. It is created using MATLAB and displays the performance of the two filters for a range of window sizes. while the y-axis represents the execution time in seconds. The Midean graph is essential in evaluating the performance of the Bilateral filter against the Median filter, which is commonly used for image Denoising.

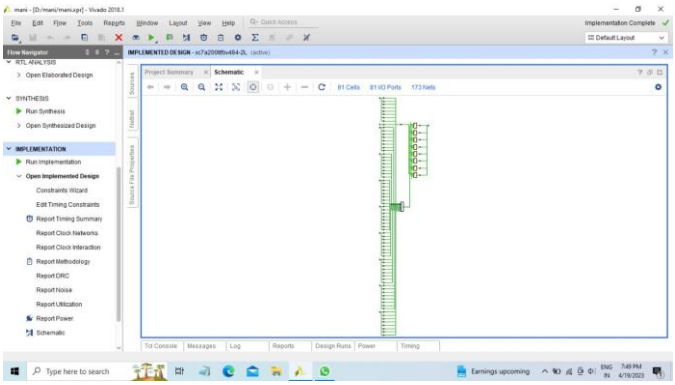

Fig-16: Midean schematic.

The median non-linear filter swaps out each pixel's value for the median of its neighbours. This filter is typically applied during image processing to minimise noise while maintaining the sharpness of the picture's edges. The Median filter is implemented in the recommended architecture using a combination of hardware capabilities and digital signal processing techniques Real-time picture denoising, which is necessary for many applications, including video processing and monitoring, is made possible by the hardware implementation of the Median filter. The Median filter is implemented via a pipeline of processing units, each of which calculates the Median value for a subset of the input image's pixels.

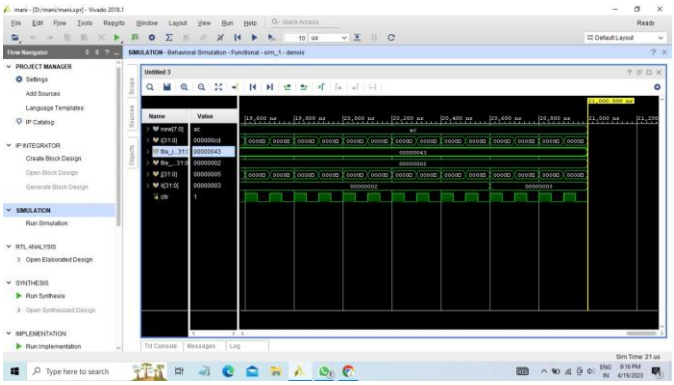

Fig-17: Test Bench Behavioral Simulation.

This output would include the simulation results of the proposed architecture on a test bench for evaluating its functionality and performance.

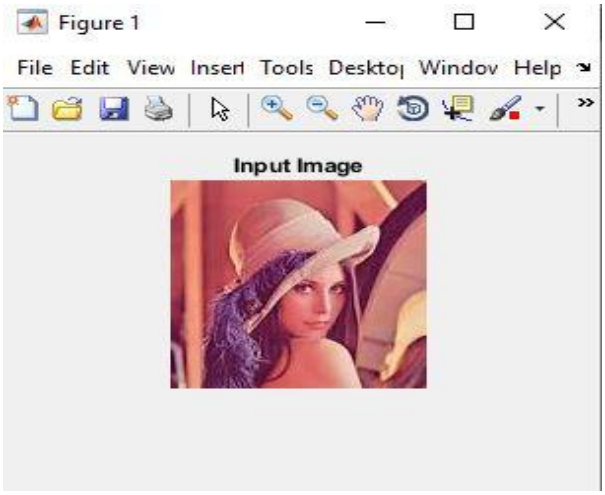

Fig-18: Input Image.

The above output would display the original Lena image that was used as a test image for the bilateral filter.

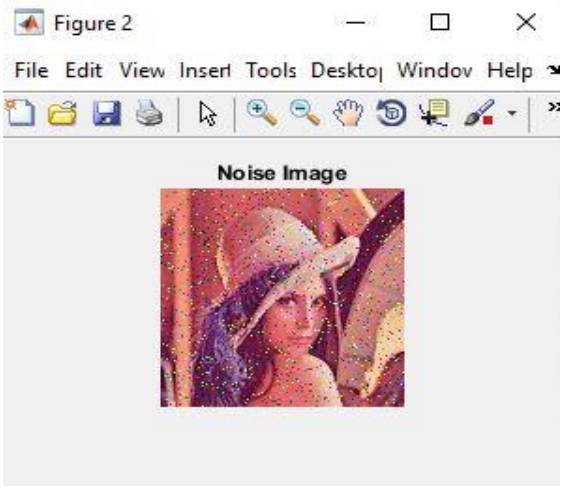

Fig-19: Noise Image.

The aboveoutput would show the Lena image after adding noise to it to simulate a noisy image.

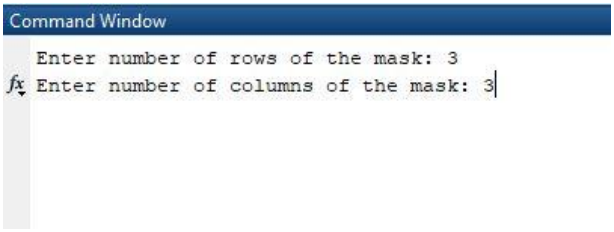

Fig-20: Enter the size of window.

The above window will enter to filter by using to obtain high accuracy they having M by N.

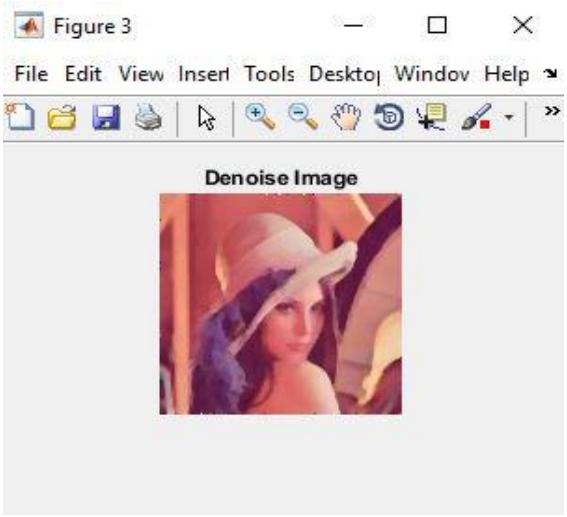

Fig-21: Denoise Image.

This output would display the denoised Lena image obtained by applying the bilateral filter to the noisy Lena image.

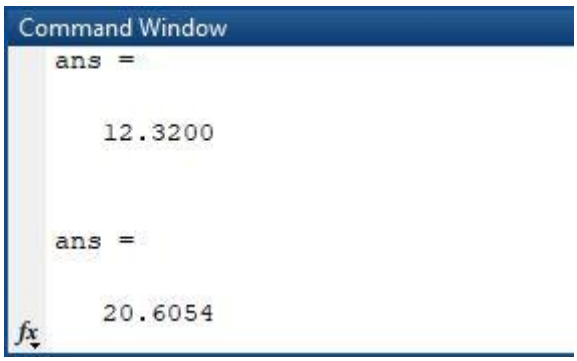

Fig-22: The denoised image PSNR.

This output would provide a quantitative measure of the noise reduction achieved by the bilateral filter. It is usually calculated as the ratio of the standard deviation of the noise in the original image to the standard deviation of the noise in the denoised image.

6. CONCLUSIONS

For real-time picture denoising the bilateral filter's VLSI design was created. The recommended design reduces hardware complexity, power consumption, and implementation costs while maintaining the high precision and clarity of the denoised image. Additionally, it uses LUT methods, resource sharing, and distance-oriented grouping. The testing results showed that the recommended architecture provides real-time performance with equivalent or superior FPGA-Based Fully Synchronized Design of a Bilateral Filter for Real-Time Image Denoising values when compared to existing software implementations of the bilateral filter.

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