

Performance Analysis of Nine level inverter with Battery Balancing Function

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Abstract - This paper deals with a single-phase nine-level cascaded inverter featuring Sinusoidal Harmonic Elimination Pulse Width Modulation (SHE PWM) along with battery balancing discharge capabilities. To optimize battery pack performance, an approach is implemented that prioritizes activation of the H-bridge associated with the battery with the maximum voltage, in descending order of battery voltage levels. This strategic sequencing significantly improves the battery pack's overall discharge efficiency. Thereby resulting in an increase in inverter efficiency. In addition to that, the optimized switching angle helps in the mitigation of harmonic distortion. The proposed system is simulated by MATLAB/Simulink. In the practical implementation of the prototype, gate triggering pulses and the battery-balanced discharge functionality are controlled by an 8-bit PIC microcontroller, PIC16F87XA model.

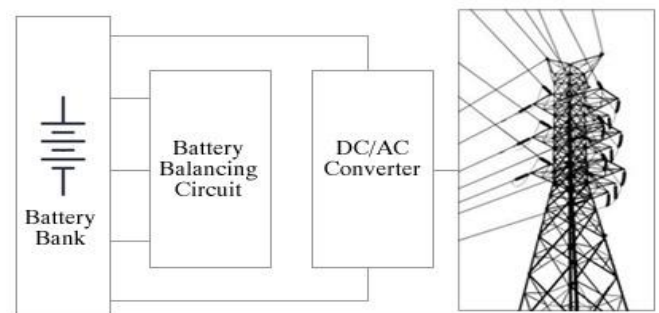


Fig -1: General Block Diagram

Key Words: Nine-level inverter, H-bridge, Battery balanced function, Harmonics, Lion optimization

1. INTRODUCTION

The rapid depletion of fossil fuels has increased interest in renewable energy sources. However, renewables are characterized by a high degree of intermittency. Utilizing a battery-based energy storage system is effective for assuring a constant and uninterrupted power supply [1]-[3].

When it comes to grid connection, various inverter topologies, including central inverters, string inverters, and microinverters, are commonly employed [4]. The cascaded multilevel inverter is one of the superior topologies. Scalability is a notable advantage of the cascaded multilevel H-bridge inverter. By adding more H-bridge modules to the cascade, the output voltage quality can be improved by adding more voltage levels to the output waveform. This scalability makes it ideal for grid-connected renewable energy systems, motor drives, and uninterruptible power supplies where high-voltage, high-power, and low-harmonic distortion requirements are essential [5]. The general block diagram is shown in Figure 1.

Individually, each inverter makes the connection to individual batteries in cascaded topology. A methodical the strategy of sorting batteries by voltage and activating

full bridges in descending voltage order significantly increase the discharge duration and overall performance of battery packs. The absence of such a balancing system results in a rapid degradation of battery discharging capacity. To improve battery storage, several battery charging strategies are mentioned in the literature reviews [6]-[8]. Adding a battery-balancing circuit will increase the complexity and cost of the circuit at the same time reduces its efficiency. As a solution, a single-phase multilevel inverter with a battery-balanced discharging function is proposed here. In addition, using a genetic algorithm, we optimize the switching angles in order to minimize total harmonic distortion in the AC output voltage.

2. CIRCUIT OPERATION

Figure 2 depicts the individual full bridge inverter and Table 1 gives its switching sequences. As shown in Figure 4, the cascaded multilevel H-bridge inverter consists of multiple H-bridge modules connected in series. Each H-bridge module includes a separate battery and two pairs of switches. By modulating the states of these switches, the inverter can generate a staircase-like output voltage waveform with multiple voltage levels, as depicted in Figure 3. These levels are typically symmetric with respect to the zero-voltage reference point, which helps achieve reduced total harmonic distortion in the output waveform. The output voltage of the multilevel inverter corresponds to the cumulative voltages of the full-bridge inverters.

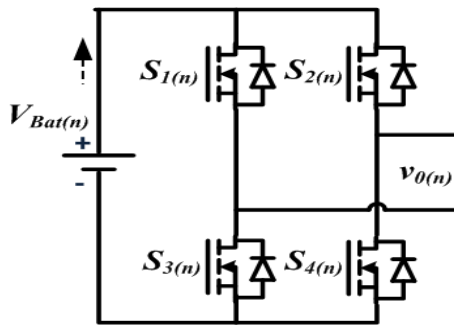


Fig -2: Individual Full Bridge Inverter

Table -1: Switching Sequence of Individual Full Bridge

Output Voltage, V_o	Switching Sequence			
	$S_{1(n)}$	$S_{2(n)}$	$S_{3(n)}$	$S_{4(n)}$
+Vdc	0	1	0	1
0	1	1	0	0
	0	0	1	1
-Vdc	1	0	1	0

In a single-phase nine-level cascaded inverter configuration, each H-bridge module is connected to a separate battery source and generates -Vdc, 0, and +Vdc voltage levels. The voltages of these individual battery cells have fluctuated over time. Battery having the highest voltage will take a longer discharge duration, whereas the battery having the lowest voltage will experience the opposite effect [10].

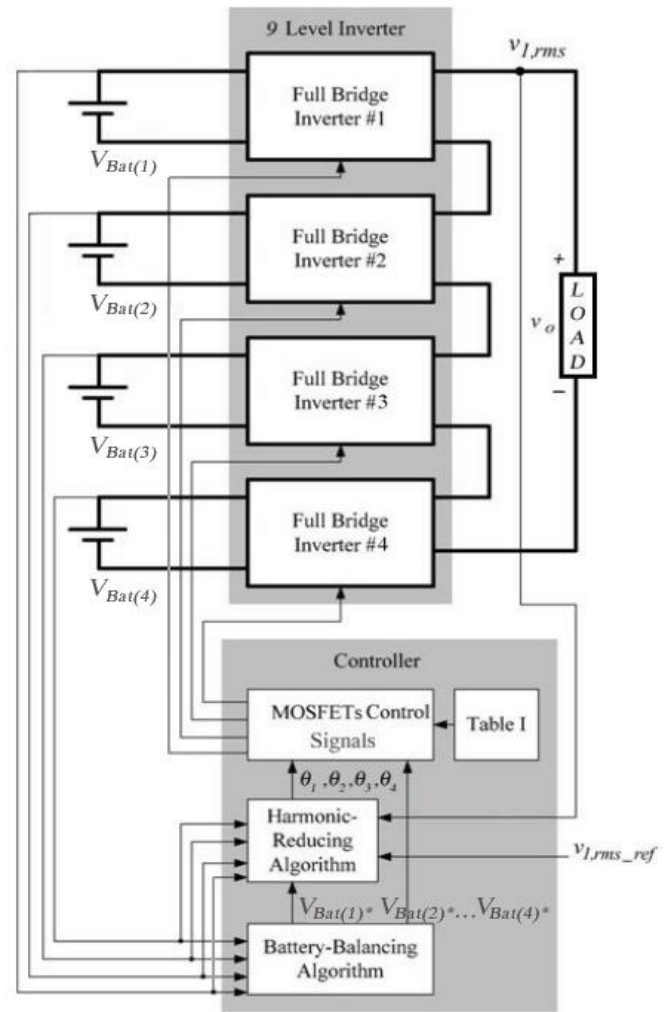


Fig -4: Nine Level Inverter with Controller

where $V_{Bat(n)}$ is the battery voltage of n^{th} battery.

The battery voltage of each full bridge can be assessed and listed as

$$V_{Bat} = \{V_{Bat(1)}, V_{Bat(2)}, \dots, V_{Bat(N)}\} \tag{2}$$

Due to manufacturing tolerances, identical battery types exhibit cell-to-cell variation. Therefore, measure the battery voltages and arrange them in descending order as shown

$$V_{Bat(sort)} = \{V_{Bat(1)*}, V_{Bat(2)*}, \dots, V_{Bat(N)*}\} \tag{3}$$

where $V_{Bat(1)*}$ = Highest battery voltage

$V_{Bat(1)*}$ = Second highest battery voltage

$V_{Bat(N)*}$ = Lowest battery voltage

The battery having a higher voltage has the potential to deliver power for a longer duration than the battery having a lower voltage. If the battery voltages are organized in the decreasing value of battery voltages,

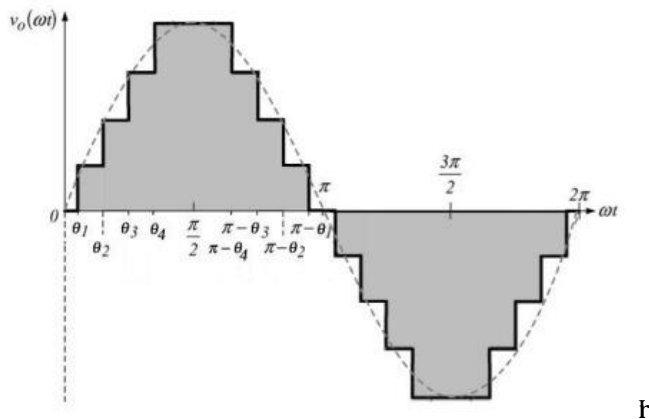


Fig -3: Output Voltage of Nine Level Inverter

In the cascaded H bridge inverter, the output voltage denoted as v_0 is determined by the cumulative sum of the individual voltages of each full-bridge inverter.

$$v_0 = \sum_{n=1}^N V_{Bat(n)} \tag{1}$$

$$V_{Bat(sort)} = \{V_{Bat(1)} * \geq V_{Bat(2)} * \geq \dots, V_{Bat(N)} *\} \quad (4)$$

then the discharging capacity of the batteries are related like this

$$Q_{Bat(sort)} = \{Q_{Bat(1)} * \geq Q_{Bat(2)} * \geq \dots, Q_{Bat(N)} *\} \quad (5)$$

It is a well-established fact that batteries with higher voltages consistently exhibit superior discharging capacities compared to the battery with lower voltages. Therefore, by initially activating the battery with the highest voltage, a longer duration of operation can be obtained. Consequently, a balanced battery discharged function can be implemented.

The full-bridge converter corresponding to the highest battery voltage, $V_{Bat(1)}$ * will initiate operation at first instant in a switching period, T_s , at a switching angle, θ_1 . Therefore, it will operate for an extended period of time. Likewise, the full-bridge converter for the second-highest battery voltage, $V_{Bat(2)}$ * will initiate operation at a switching angle of θ_2 . Consequently, the H bridges are activated in decreasing battery voltage values.

The output voltage of the multilevel inverter with distinct DC sources can be expressed as

$$v_0 = V_{Bat(1)} * + V_{Bat(2)} * + \dots + V_{Bat(N)} * \quad (6)$$

The output waveform of cascaded H bridge will be in the form of staircase or stepped in nature as shown in Figure 4. The Fourier Series of staircase or stepped output waveform is given by

$$v_{\omega t rms} = \frac{4}{\sqrt{2n\pi}} (V_{Bat(1)} * \cos(n\theta_1) + V_{Bat(2)} * \cos(n\theta_2) + \dots + V_{Bat(N)} * \cos(n\theta_N)) \sin(n\omega t) \quad (7)$$

where n is the order of harmonics
N denotes the number of DC sources

3. OPTIMIZATION TECHNIQUE USED

The selection of switching angles for the inverter is undertaken with the objective of minimizing the total harmonic distortion (THD) value [11]-[14]. To attain this objective, it is necessary to examine the following harmonic equations.

$$v_{1 rms} = \frac{4}{\sqrt{2\pi}} (V_{Bat(1)} * \cos(\theta_1) + V_{Bat(2)} * \cos(\theta_2) + V_{Bat(3)} * \cos(\theta_3) + + V_{Bat(4)} * \cos(\theta_4) \quad (8)$$

$$v_{3 rms} = \frac{4}{\sqrt{2 3\pi}} (V_{Bat(1)} * \cos(3\theta_1) + V_{Bat(2)} * \cos(3\theta_2) + V_{Bat(3)} * \cos(3\theta_3) + + V_{Bat(4)} * \cos(3\theta_4) \quad (9)$$

$$v_{5 rms} = \frac{4}{\sqrt{2 5\pi}} (V_{Bat(1)} * \cos(5\theta_1) + V_{Bat(2)} * \cos(5\theta_2) + V_{Bat(3)} * \cos(5\theta_3) + + V_{Bat(4)} * \cos(5\theta_4) \quad (10)$$

$$v_{7 rms} = \frac{4}{\sqrt{2 7\pi}} (V_{Bat(1)} * \cos(7\theta_1) + V_{Bat(2)} * \cos(7\theta_2) + V_{Bat(3)} * \cos(7\theta_3) + + V_{Bat(4)} * \cos(7\theta_4) \quad (11)$$

$$\text{where } 0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \frac{\pi}{2}$$

According to selective harmonic elimination [9], choose $v_{1 rms}$ is equivalent to the fundamental component, while simultaneously reducing the presence of harmonic components such as the third, fifth, and seventh harmonics to minimum.

$$v_{1 rms} = v_f \quad (12)$$

$$v_{3 rms} = v_{5 rms} = v_{7 rms} = 0 \quad (13)$$

In order to optimize the THD value, the Genetic Algorithm is employed here. In GA, a few random switching angles are selected as generation and population indices are computed. The objective function is computed within the constraints to find out the best values after iterations. Equations (8) to (13) provide the values of switching angles. Determine the minimized fitness function (THD) based on this information.

4. SIMULATION RESULTS

Figure 5 shows the simulation model of nine level inverter at instant t_1 .

At time $t = t_1$, the battery voltages are $V_{Bat1} = 8.2V$, $V_{Bat2} = 7.6V$, $V_{Bat3} = 7.5V$, and $V_{Bat4} = 7.9V$. Batteries are sorted in descending order of their voltages by comparing their voltages,

$$V_{Bat1} > V_{Bat4} > V_{Bat2} > V_{Bat3}$$

The sorted battery sequence is therefore denoted as

$$V_{Bat sort} = \{V_{Bat1}, V_{Bat4}, V_{Bat2}, V_{Bat3}\}$$

It is essential to remember that batteries with higher voltages have a greater discharge capacity. Consequently, the full bridge is switched beginning with the battery having the highest voltage, then the battery having the second-highest voltage, and so on. The sequential switching angles are $\theta_1 < \theta_4 < \theta_2 < \theta_3$, resulting in a balanced battery discharge function.

Figure 6 illustrates the FFT analysis and Figure 7 gives the output voltage of a nine-level inverter.

Figure 8 illustrates the simulation model of a nine-level inverter with a battery balanced discharging function, while Figure 9 depicts the FFT analysis and Figure 10 shows the output voltage at that time $t = t_2$.

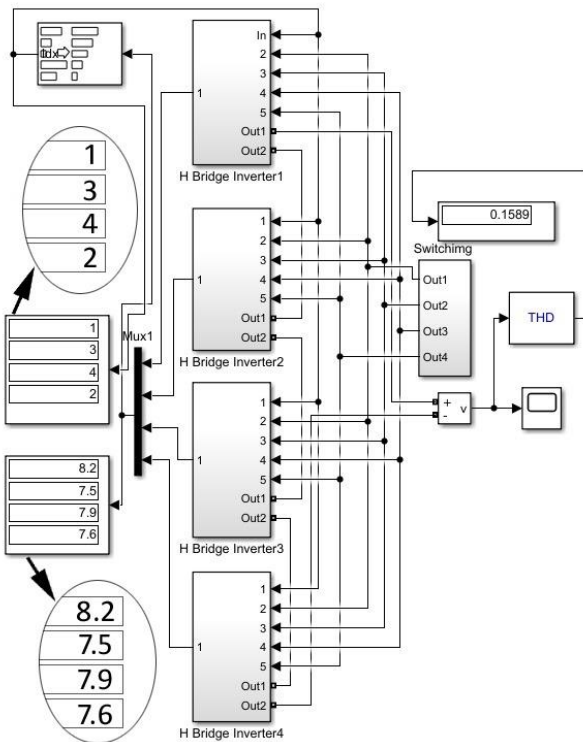


Fig -5: Simulation Model with Battery Balanced Discharge Function at t_1

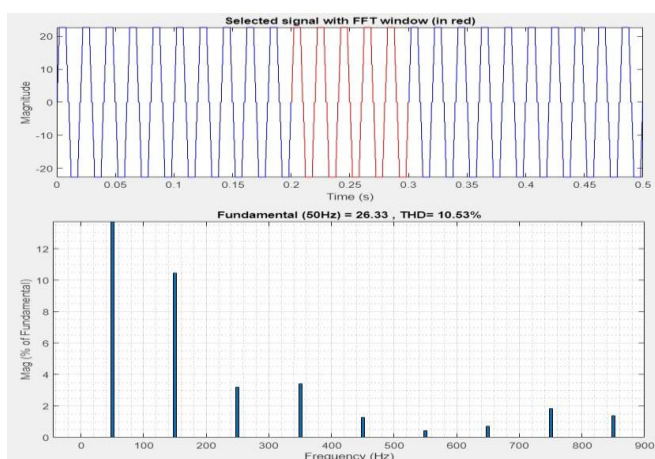


Fig -6: FFT analysis at t_1

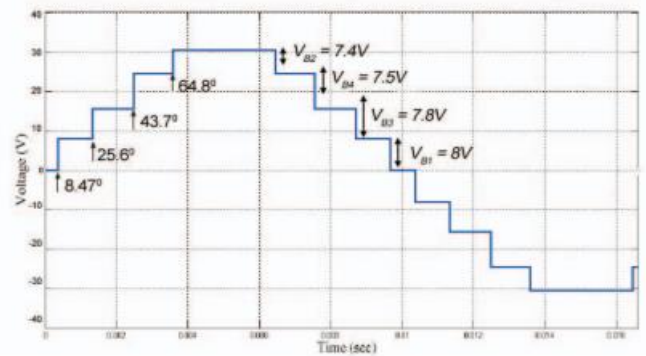


Fig -7: Output step waveform at t_1

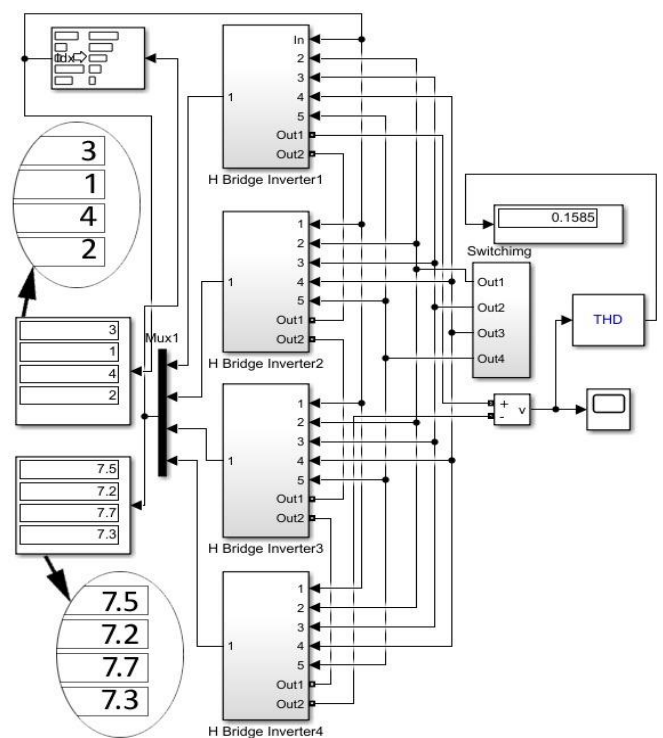


Fig -8: Simulation Model with Battery Balanced Discharge Function at t_2

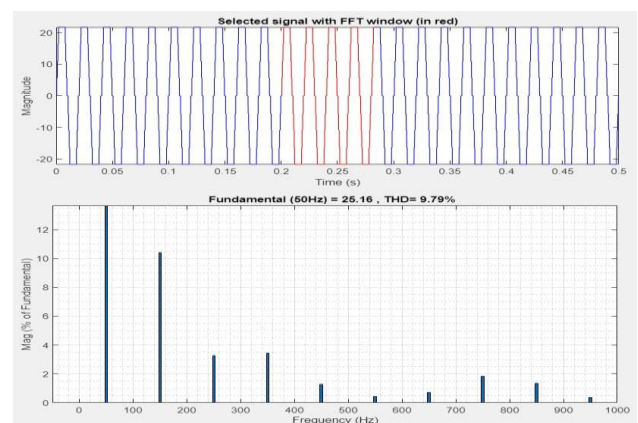


Fig -9: FFT analysis at t_2

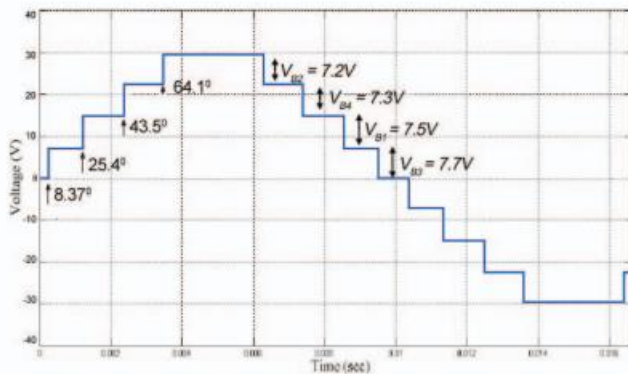


Fig -10: Output step waveform at t_2

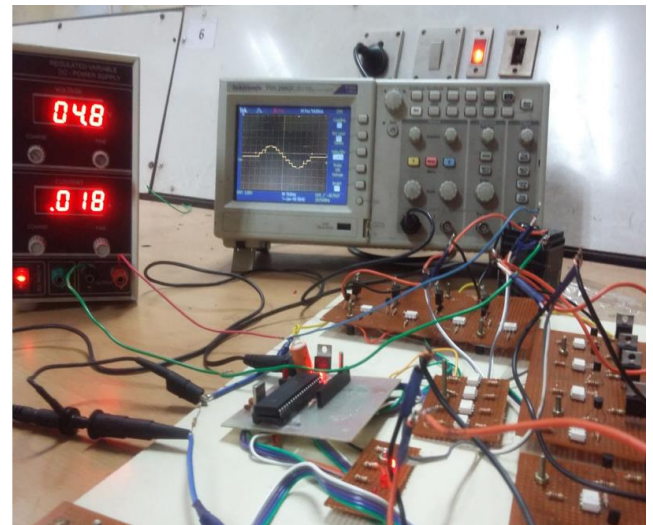


Fig -13: Hardware setup

5. HARDWARE IMPLEMENTATION AND RESULTS

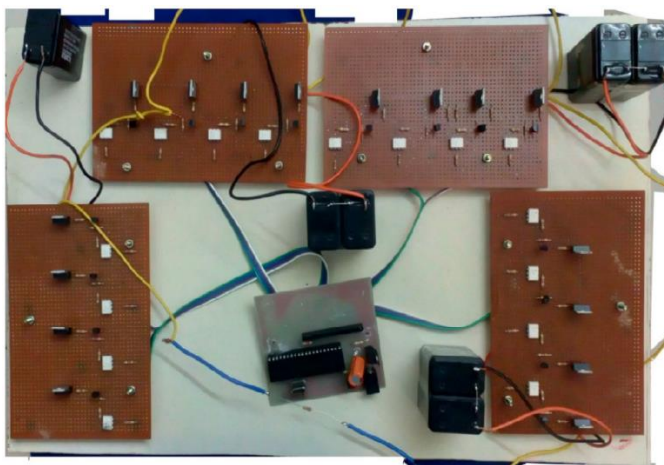


Fig -11: Hardware implementation of prototype

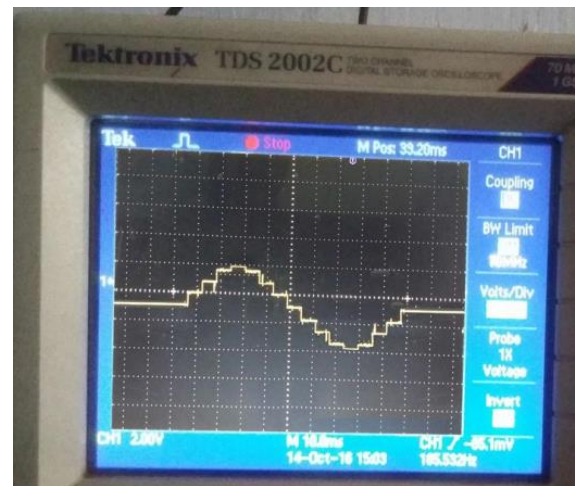


Fig -14: Output step waveform



Fig -12: Control Circuit

Figure 11 shows the hardware prototype of a nine-level inverter. The input from each inverter is directly connected to a battery. Four batteries having 8V and 0.5Ah are used. IRFPZ44N MOSFET is used as the switches in the full bridge and the MCT2E optocoupler is also used in the gate triggering circuit. 8-bit PIC microcontroller PIC16F87XA is used here for gate triggering pulses and battery-balanced discharging function. Figure 12 depicts the control circuit.

The frequency of the output is assumed to be 50 Hz. GA is used to find out the inverter's switching angles. These switching angles are fed into a look-up table and loaded into a microcontroller. As per the sorting order of batteries, the inverter's switching angles are given by the microcontroller. One 8V battery is replaced with a 4V battery to check the battery balancing. According to the battery balanced discharging function, batteries are sorted as per the decreasing values of battery voltages and first turn on the full bridge having the highest battery voltage and so on. Also, one or two batteries can be replaced with a variable DC source. Then by varying the DC source, we can check the battery balanced discharging function. The hardware implementation circuit is shown in Figure 13. Figure 14 represents the result as shown in the oscilloscope.

6. CONCLUSIONS

The Nine-Level Cascaded Inverter having individual DC sources is designed for checking battery balanced discharge

function. Optimization by Genetic Algorithm helps to achieve the lowest possible THD by selective harmonic elimination technique. It provides the switching angles corresponding to minimum THD. The batteries are arranged in descending order of their voltages, and the full bridges are switched on accordingly. Thus, the algorithm for balanced battery discharge is obtained. This optimized approach extends the battery backup duration, thereby enhancing the overall efficiency of the inverter. The feasibility of the proposed system has been experimentally validated. The primary benefit of the system is the utilization of a simple PIC microcontroller for its controller, and it is a cost-effective solution.

REFERENCES

- [1] B. P. Roberts and C. Sandberg, "The Role of Energy Storage in Development of Smart Grids," in Proceedings of the IEEE, vol. 99, no. 6, pp. 1139-1144, June 2011, doi: 10.1109/JPROC.2011.2116752.
- [2] S. Ould Amrouche, D. Rekioua, T. Rekioua, S. Bacha, "Overview of energy storage in renewable energy systems", International Journal of Hydrogen Energy, Volume 41, Issue 45, 2016, Pages 20914-20927, ISSN 0360-3199, <https://doi.org/10.1016/j.ijhydene.2016.06.243>.
- [3] D. Parra, M. Swierczynski, D.I. Stroe, Stuart.A. Norman, A. Abdon, J. Worlitschek, T. O'Doherty, L. Rodrigues, M. Gillott, X. Zhang, C. Bauer, M. K. Patel, "An interdisciplinary review of energy storage for communities: Challenges and perspectives", Renewable and Sustainable Energy Reviews, Volume 79, 2017, Pages 730-749, ISSN 1364-0321, <https://doi.org/10.1016/j.rser.2017.05.003>.
- [4] Salem, M.; Richelli, A.; Yahya, K.; Hamidi, M.N.; Ang, T.-Z.; Alhamrouni, I. A Comprehensive Review on Multilevel Inverters for Grid-Tied System Applications. Energies 2022, 15, 6315. doi:10.3390/en15176315
- [5] M. Annoukoubi, A. Essadki and T. Nasser, "Cascade H-Bridge Multilevel Inverter for a Wind Energy Conversion System Applications," 2021 9th International Renewable and Sustainable Energy Conference (IRSEC), Morocco, 2021, pp. 1-7, doi: 10.1109/IRSEC53969.2021.9741171.
- [6] C. Sen and N. C. Kar, "Battery pack modeling for the analysis of battery management system of a hybrid electric vehicle," 2009 IEEE Vehicle Power and Propulsion Conference, Dearborn, MI, USA, 2009, pp. 207-212, doi: 10.1109/VPPC.2009.5289848.
- [7] M. Shousha, T. McRae, A. Prodić, V. Marten and J. Milios, "Design and Implementation of High Power Density Assisting Step-Up Converter With Integrated Battery Balancing Feature," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 3, pp. 1068-1077, Sept. 2017, doi: 10.1109/JESTPE.2017.2665340.
- [8] F. Eroğlu and A. M. Vural, "A Critical Review on State-of-Charge Balancing Methods in Multilevel Converter Based Battery Storage Systems," 2022 4th Global Power, Energy and Communication Conference (GPECOM), Nevsehir, Turkey, 2022, pp. 14-19, doi: 10.1109/GPECOM55404.2022.9815810.
- [9] C. Buccella, C. Cecati, M. G. Cimatoroni and K. Razi, "Analytical Method for Pattern Generation in Five-Level Cascaded H-Bridge Inverter Using Selective Harmonic Elimination," in IEEE Transactions on Industrial Electronics, vol. 61, no. 11, pp. 5811-5819, Nov. 2014, doi: 10.1109/TIE.2014.2308163.
- [10] Chung-Ming, Neng-Yi Chu, Liang-Rui Chen, Yu-Chih Hsiao, and Chia Zer Li "A Single-Phase Multilevel Inverter With Battery Balancing," IEEE Trans. on Industrial Electronics, Vol. 60, No. 5, May 2013
- [11] K. F. Man, K. S. Tang, and S. Kwong, "Genetic algorithms: Concepts and applications in engineering design," IEEE Trans. Ind. Electron, vol. 43, no. 5, pp. 519-534, Oct. 1996.
- [12] R.Vijayakumar, Alamelu Natchiappan, C. Devialitha, R. Mazhuventhi "Selective Harmonic Elimination PWM Method using Seven Level Inverters by Genetic Algorithm Optimization Technique," International Journal of Engineering Research & Technology (IJERT) ISSN: 2278- 0181 Vol. 4 Issue 02, February-2015.
- [13] S. Joseph and C. A. Babu, "Performance analysis of multilevel inverter with battery balanced discharge function and harmonic optimization with genetic algorithm," 2016 International Conference on Next Generation Intelligent Systems (ICNGIS), Kottayam, India, 2016, pp. 1-6, doi: 10.1109/ICNGIS.2016.7854068.
- [14] Hajizadeh, Mehdi, Fathi, Seyed Hamid, "Selective harmonic elimination strategy for cascaded H-bridge five-level inverter with arbitrary power sharing among the cells", IET Power Electronics, VL - 9, IS SN - 1755-4535, <https://doi.org/10.1049/iet-pel.2014.0966>

BIOGRAPHIES

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