

# SIMULATION STUDY OF DIELECTRIC MODULATED DUAL-MATERIAL TRI GATE JUNCTIONLESS FET BASED BIOSENSOR

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**Abstract** - This manuscript explores the simulation of a tri-gate Junctionless Accumulation Mode Field-Effect Transistor (JLAM-FET) in Silvaco, conducting an analysis to calculate sensitivity while varying permittivity concerning shifts in parameters such as threshold voltage, charge, doping concentration, and channel length, specifically in the context of biomolecules. Unlike a traditional Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), a junctionless transistor lacks junctions, and its current drive is regulated by doping concentration rather than gate capacitance. Notably, a Junctionless transistor exhibits superior performance compared to a conventional MOSFET, particularly in scenarios with a short channel length. An optimal doping concentration of  $1 \times 10^{18} \text{ cm}^{-3}$  and a threshold voltage change of 2000 mV are identified to achieve maximum sensitivity. The alteration in the central potential of the channel emerges as a critical factor in determining both threshold voltage and device sensitivity. The successful simulation of the device captures all variations and outcomes. As we navigate through the intricate landscape of semiconductor physics and biomolecular interactions, the findings not only solidify the JL AM-FET's standing as a forefront technology but also open avenues for tailoring its capabilities to specific biomolecular sensing applications. This holistic approach contributes to the growing body of knowledge in semiconductor device engineering, presenting opportunities for the development of innovative solutions in biosensing technology.

**Key Words:** Short channel effects, Central potential alteration, Current drive, Central potential alteration, Channel length, Permittivity variation, Sensitivity analysis.

## 1. INTRODUCTION

Biosensors are crucial tools for the rapid detection of biomolecules, with a particular promise in label-free detection of both neutral (biotin-streptavidin) and charged biomolecules (DNA). The advancement in fabrication technologies has facilitated the cost-effective large-scale production of nanoscale biosensors, which are compatible with CMOS (Complementary Metal Oxide Semiconductor) technology. This integration streamlines the detection systems, eliminating the need for complex transducers and paving the way for system-on-chip (SoC) applications.

Among the different types of biosensors developed, including optical, electrochemical, nano-mechanical devices, ion-sensitive electrodes, and piezoelectric models, Field Effect Transistor (FET)-based biosensors have gained widespread adoption.

Junctionless field-effect transistors (JLFETs) are emerging as promising devices due to their simpler fabrication process, which omits the need for conventional p-n junctions, enabling further device miniaturization. These transistors offer a high ION/IOFF ratio, minimal thermal budgeting, near-ideal subthreshold swing, and reduced roll-off. However, JLFETs face challenges such as mobility degradation due to heavily doped channels and reduced ON current (ION) caused by high parasitic resistances.

To address these issues, Junction Accumulation Mode (JAM) FETs have been introduced. They maintain heavy doping in the source/drain regions while lowering the channel doping, enhancing both ION and the ION/IOFF ratio compared to traditional JLFETs. However, high electric fields at the channel/drain interface during the ON state can lead to hot-electron effects (HCEs) and gate-induced drain leakage (GIDL). Dual-material gate engineering is a proven method to counteract these reliability issues, as well as short-channel effects (SCEs), in various FET architectures.

Additionally, the Tri-Gate (TG) architecture has gained attention for its excellent gate control in sub-100 nm regimes, making it highly effective in mitigating SCEs and conducting higher currents than double-gate MOSFETs (DG-MOSFETs). The feasibility of fabricating both n-channel and p-channel TG MOSFETs underscores its potential for real-world applications. Tri-Gate devices are known for their high ION/IOFF ratio and power efficiency, making them more power-efficient than other FET types, including planar or FinFETs. Features like reduced surface scattering, improved subthreshold swing (SS), and lower drain-induced barrier lowering (DIBL) make TG-JLFETs particularly suitable for both analog and digital applications. The TG-JLFET architecture's enhanced gate-channel electrostatics offer immunity to SCEs, pushing the boundaries of device scaling. With increasing demand for high packing density, managing short-channel effects and parasitic capacitances, such as those addressed by Silicon-on-Insulator (SOI) technology, becomes crucial.

### 1.1 Method of Operation

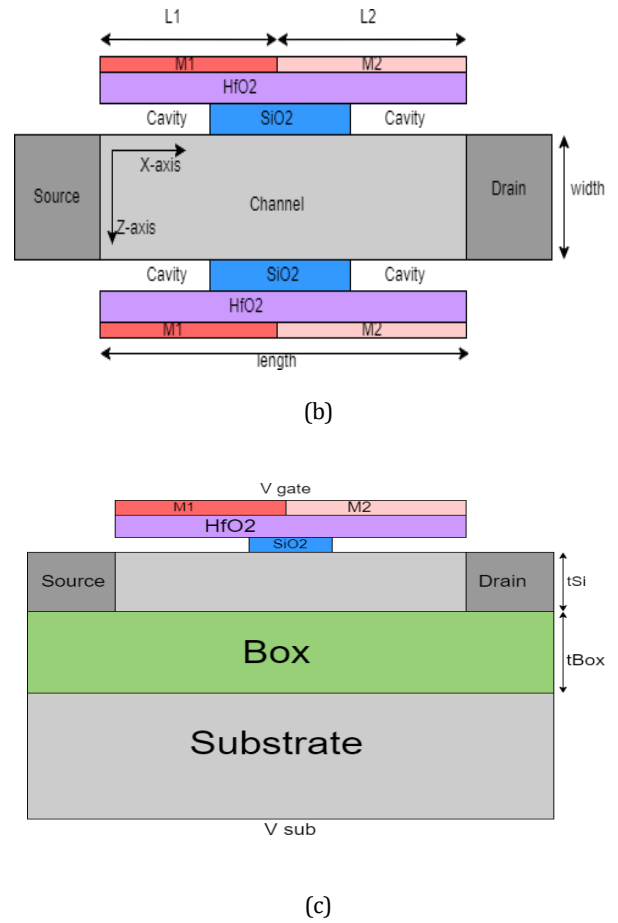
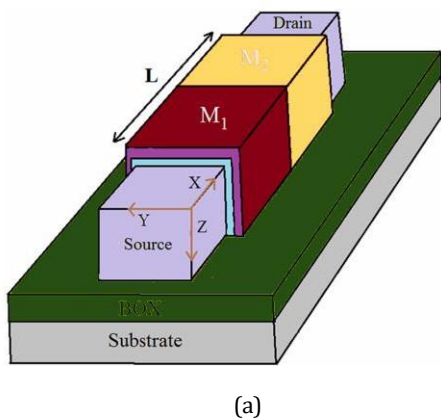
The operation of a Junctionless field-effect transistor (JL-FET) is based on the modulation of the conductive channel between the source and drain regions by the electric field applied by the gate electrode. Unlike traditional field-effect transistors (FETs), JL-FETs do not rely on a junction between different semiconductor materials for their operation. Instead, the entire channel is uniformly doped, and the gate voltage directly influences the conductivity of the channel.

### 1.2 Device Structure and Analytical Model Outline

The 3-D structure of a Tri-Gate Junctionless Field-Effect Transistor (JL FET) is illustrated in Fig. 1(a). The top view of the device, as shown in Fig. 1(b), reveals a symmetric double-gate configuration, while the side cross-sectional view, depicted in Fig. 1(c), presents the device as an asymmetric Silicon-On-Insulator (SOI) structure. The silicon film is enveloped on three sides by stacked oxide layers—HfO<sub>2</sub> on top of cavities and SiO<sub>2</sub>—with respective thicknesses  $t_{HfO_2}$  and  $t_{SiO_2}$ , maintaining an effective oxide thickness (EOT) of  $t_{OX}$ . The gate is formed using two metals with different work functions ( $\phi_{M1}$  and  $\phi_{M2}$ ). The device features varying donor densities in the channel and source/drain (S/D) regions, with the S/D regions doped at a higher level (NSD) and the channel doped at a slightly lower concentration (NC) of the same type. The channel's length, width, and thickness are oriented along the x, y, and z-axes, respectively.

The proposed device has been analytically modelled with specific geometrical constraints: i) the thickness of the buried oxide layer ( $t_{box}$ ) must be greater than or equal to the channel length ( $L$ ) to minimize interaction between the two side gates; ii) the channel length should be at least twice the width/thickness of the device or more, i.e.,  $L \geq 2W$  and  $L$

$\geq 2t_{si}$ . The channel potential [ $\psi(x,y,z)$ ] at any given point is represented using a perimeter-weighted sum approach, combining  $\psi(x,y)$  and  $\psi(x,z)$ . These are the potential functions for the symmetric double-gate structure and the asymmetric SOI device, respectively, derived from the analytical model by solving the 2D Poisson's Equation.



**Fig. 1** TG JL FET with gate stack:(a) 3-D schematic view, (b) Top cross-sectional view, (c) Side cross-sectional view

### 1.3 Device Parameters

The performance of the Dual-material Tri Gate JLFET is significantly influenced by several critical parameters. The channel length ( $L$ ) determines the distance between the source and drain regions, impacting the device's current-carrying capability and overall conductance. For effective short-channel performance, the channel length is carefully designed to be at least twice the channel width ( $W$ ) and thickness ( $t_{si}$ ), ensuring minimal interaction between the side gates. The channel width ( $W$ ) and thickness ( $t_{si}$ ) are also crucial, as they affect the electrostatic control and current flow through the channel. The gate oxide thickness ( $t_{ox}$ ) plays a pivotal role in defining the gate capacitance and control over the channel, with a balance needed between performance enhancement and gate leakage. The thickness of the buried oxide layer ( $t_{box}$ ) is chosen to be greater than or equal to the channel length to reduce the interaction between the side gates. Doping concentrations in the source and drain regions, as well as the channel, are optimized to enhance the ON current ( $I_{ON}$ ) and the  $I_{ON}/I_{OFF}$  ratio. The gate is constructed using metals with distinct work functions ( $\phi_{M1}$  and  $\phi_{M2}$ ), which influence the threshold voltage and device characteristics. Additionally, the gate oxide comprises stacked layers of high-K dielectric material (HfO<sub>2</sub>) and SiO<sub>2</sub>,

with their respective thicknesses ( $t_{HfO2}$  and  $t_{SiO2}$ ) optimized to minimize surface scattering and gate leakage while maintaining the effective oxide thickness (EOT). The orientation of channel dimensions along the x, y, and z axes affects the device's spatial characteristics and performance. Managing parasitic capacitances, often through techniques like Silicon-on-Insulator (SOI) technology, is also crucial for improving the switching speed and overall efficiency of the device. Each of these parameters plays a vital role in defining the functionality and efficiency of the device, and their careful optimization is essential for achieving high-performance Field-Effect Transistors.

All simulations are conducted using the Silvaco ATLAS device simulator, employing standard density models. The primary models utilized in the simulation include the Drift-Diffusion model, the Shockley-Read-Hall (SRH) recombination model, and the Lombardi Mobility Model. A robust meshing strategy is implemented to ensure precision. Empirical parameters incorporated into the model are sourced from references. The body (substrate) and source terminals are connected to ground to complete the circuit.

**Table -1:** Device dimensions and biasing voltages used for simulations

Parameters	Values
High-K oxide layer thickness( $t_{HfO2}$ )	2nm
Thickness of Silicon dioxide( $t_{SiO2}$ )	1nm
Work-functions of dual metal gate ( $\phi_{M1}$ , $\phi_{M2}$ )	4.7eV, 5.2eV
Channel doping (NC)	$10^{18} \text{ cm}^{-3}$
Channel length (L)	30nm
Source/Drain doping (NSD)	$10^{20} \text{ cm}^{-3}$
Thickness of the buried oxide layer ( $t_{box}$ )	60nm
Thickness and width of Si-film ( $t_{Si}$ , W)	10nm, 10nm
Gate voltage ( $V_{gs}$ ), Drain Voltage ( $V_{ds}$ )	0-2V, 0.8V

## 2.SENSITIVITY ANALYSIS

Sensitivity is a crucial parameter to consider while evaluating a biosensor's effectiveness. The Dual-material tri gate JLFET's sensitivity is assessed based on changes in electrical characteristics (I & V) brought on by variations in the target biomolecule's relative dielectric constants to the air in the nanogap cavity. In this work the threshold voltage sensitivity ( $S_{V_{th}}$ ) is taken into account to assess its performance. And it can be calculated as:

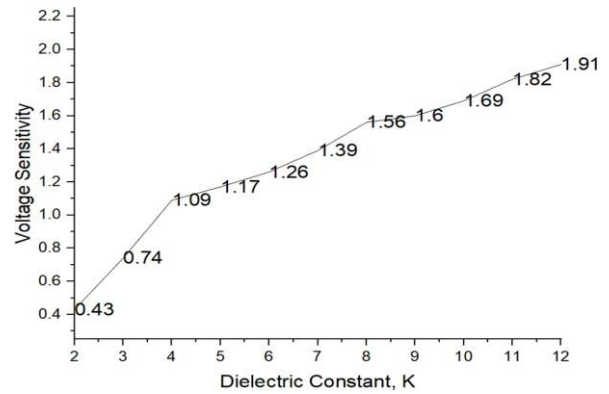
$$S_{V_{th}} = \frac{V_{th(bio)} - V_{th(air)}}{V_{th(air)}}$$

where,

$V_{th(bio)}$ - Threshold voltage for a certain biomolecule in the cavity

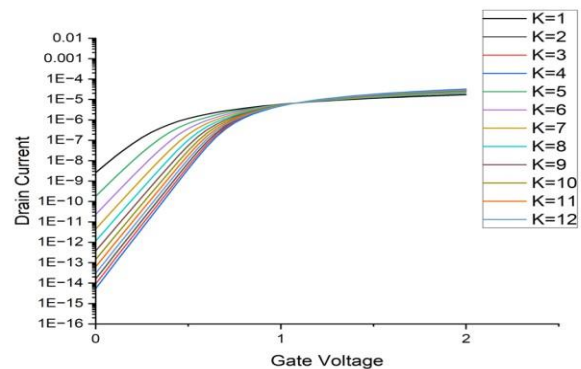
$V_{th(air)}$ - Threshold voltage for air in the cavity

### 2.1 Result



**Fig.2(a):** Voltage Sensitivity along the changing dielectric constant

Figure 2(a) clearly demonstrates that an increase in the dielectric constant within the nanogap cavity region results in a significant enhancement in the voltage sensitivity of the device. This observation underscores the critical role that the dielectric environment plays in determining the device's sensitivity to voltage changes. As the dielectric constant within the nanogap cavity is increased, the device exhibits a marked improvement in its voltage sensitivity, which directly influences its ability to detect and respond to minute variations in electrical signals. This enhanced sensitivity is particularly important for applications requiring precise measurement and detection, as it enables the device to discern smaller changes in voltage more effectively. The relationship between the dielectric constant and voltage sensitivity highlighted in the figure illustrates the potential for optimizing device performance through adjustments in the dielectric environment, ultimately leading to improved accuracy and reliability in its sensing capabilities.



**Fig.2(b):** Drain Current VS Gate Voltage

Figure 2(b) illustrates that an increase in the dielectric constant within the nanogap cavity region of the device leads to a corresponding rise in the threshold voltage. This effect is crucial in understanding how variations in the dielectric environment impact the performance of the Junctionless FET-based biosensor. Specifically, when the dielectric constant ( $K$ ) is altered, the device's threshold voltage changes significantly. In the context of the biosensor's optimal doping concentration, set at  $1 \times 10^{18} \text{ cm}^{-3}$ , the change in threshold voltage is notably pronounced. For dielectric constants of  $K$ -filled = 1 and  $K$ -filled = 12, the threshold voltage variation amounts to 400 mV. This substantial shift highlights the sensitivity of the device to changes in the dielectric environment, which is a critical factor in enhancing the biosensor's detection capabilities. The ability of the device to exhibit such a pronounced response to dielectric changes underlines its potential for precise biomolecule sensing applications, where even minor variations in the dielectric constant can be detected and quantified. This characteristic makes the Junctionless FET-based biosensor a promising tool for advanced sensing technologies, where high sensitivity and accuracy are essential.

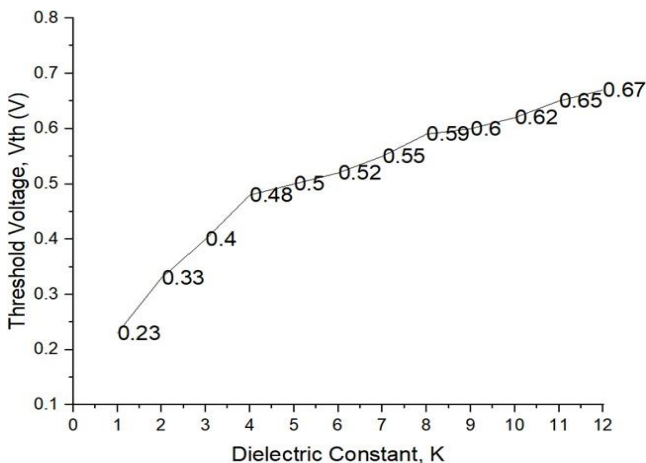


Fig.2(c): Threshold Voltage VS Dielectric Constant

It can be seen that  $V_{TH}$  increases with rise in  $k$  due to reduction in  $ID$ . It is observed that the proposed biosensor gives better discrimination among biomolecules at lower values of  $k$  whereas the discriminability of sensor sharply decreases with increase in  $k$ . This is due to the fact that the change in  $V_{TH}$  is lesser for higher values of  $k$ . Therefore, the proposed biosensor is highly selective for lower values of  $k$ .

### 3.CONCLUSIONS

In this study, we investigated the performance of a Dual-material tri gate JLFET for biomolecule sensing, utilizing simulations conducted in the Silvaco ATLAS device simulator. Our analysis focused on how variations in dielectric constant within the nanogap cavity affect critical parameters such as threshold voltage and voltage sensitivity.

The findings revealed that an increase in dielectric constant significantly enhances both the threshold voltage and voltage sensitivity, demonstrating the device's potential for high-sensitivity biomolecule detection.

The Dual-material tri gate JLFET design, characterized by an optimal doping concentration of  $1 \times 10^{18} \text{ cm}^{-3}$ , exhibited a notable change in threshold voltage, when transitioning from dielectric constants of  $K$ -filled = 1 to  $K$ -filled = 12. This substantial sensitivity to dielectric changes underscores the device's suitability for applications requiring precise detection of biomolecular interactions. Furthermore, the implementation of robust meshing strategies and standard density models, including the Drift-Diffusion model, SRH recombination model, and Lombardi Mobility Model, ensured accurate simulation results.

Overall, the Dual-material tri gate JLFET presents a promising platform for label-free biosensing, offering significant advantages in sensitivity and simplicity over traditional biosensors. The study highlights the importance of optimizing dielectric environments and device parameters to achieve enhanced performance in semiconductor-based biosensors. Future work could explore further refinement of the device structure and the integration of additional sensing modalities to expand its applicability in biomedical and environmental monitoring.

### ACKNOWLEDGEMENTS

We would like to thank the Department of Electronics and Communication Engineering, G.B Pant Institute of Engineering and Technology Pauri for their constant support.

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