Design and implementation of step-down Forward converter for dual output

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Abstract - *power supply module (PSM) is widely used in modern power electronics to deliver power to the different applications. In this paper, the use of forward converter topology to design step-down dc-dc converter with the help of transformer (to provide isolation between the input and the output) is proposed for application that require low output ripple, high output current and high conversion ratio. The proposed converter uses new generation SiC MOSFET's in parallel that have good efficiency and better conduction losses. The operating principle and design producers are presented together with analysis. The selected topology provides a better conversion with less ripple voltage at the output, by which the overall energy stored in the inductor can be decreased and/or increase the efficiency of the converter. The circuit is provided with under voltage protection for which the converter shuts down below the minimum voltage. The converter operation is validated for 80W with 5V/8A for each output, which is simulated in LT-SPICE & hardware is successfully tested at 150KHz operating frequency.*

Key Words:* power supply module (PSM), *forward converter, high step-down dc-dc converter, under voltage protection, operating frequency

1. INTRODUCTION

Power supply module is an interface between power source and the electronic load. The primary purpose of the power supply unit is to modulate or convert the available electrical energy from the power supply into the form required by the load [1]. It is quite rare that the power source directly matches the requirements of a particular load. So, the power supply units find extensive applications that play a crucial part in modern power electronics (like battery operated devices, power supply design, renewable energy system, etc.) that require high conversions ratio. Typically, a high step-down transformer with isolated Pulse-Width-Modulation (PWM) IC plays a major part in the voltage conversion [2-4].

DC/DC converters are known as power converters that convert electrical power provided from a source at a certain voltage level to electrical power at a different level, often providing a regulated output. Various applications like power supplies for computers, various consumer electronic goods, uninterrupted power supplies [UPS], telecommunication units and so on by the DC/DC converters. Regulated DC power supplies are required for better and efficient operation of electronic systems. Most of the power supply are designed to meet the basic requirements like regulated output, electrical isolation and multiple outputs. In addition to these basic requirements, common goals of any power supply design are to reduce the size, weight and to increase efficiency [5-7].

The use of SiC MOSFET's in parallel provides the converters topology with good current handling capacity with the benefits of faster switching characteristics and lower on-state resistance, leading to improved efficiency. The main benefit of the forward converter topology is its increased efficiency over other topologies as a result of lower switching and conduction losses. Electrical isolation between input and output stage is necessary for application where safety is paramount [8].

The transformer used in the converter is modelled with magnetizing inductance and dependent sources. By implementing forward converter with wide input range, the current distribution across the parallel MOSFET's, high efficiency, low switching losses etc, is achieved [9]. The converter is applicable with the benefits in medium to high power application with the power rating of less than 200W and which require high efficiency with optimal switching condition [10]. The block diagram of the forward dc-dc converter as shown in Fig-1.

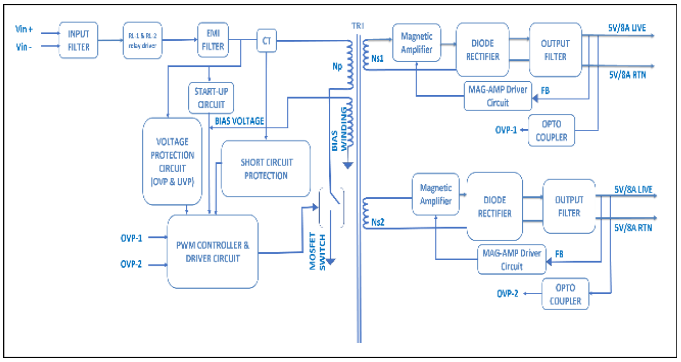

Fig-1 Block diagram

The rest of the paper is organized as follows. The topology is described and analyzed in Section II. The specification and design is provided in Section III. The experimental results are given in Section IV. Finally, Section V concludes this paper.

2. TOPOLOGY SELECTION AND PRINCIPLE OF OPERATION

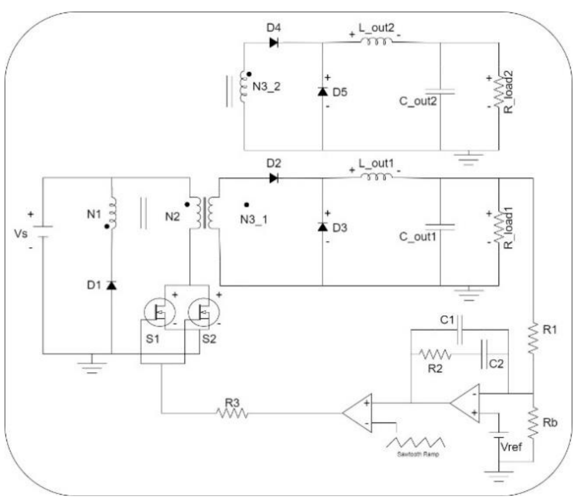

Fig-2 proposed topology

2.1. Topology selection:

The proposed converter for the application consists of a forward converter with a parallel MOSFET's and dual output is shown in Fig-2.

Derived from the buck topology, the single MOSFET forward converter employs a transformer that helps to provide galvanic isolation as well as voltage step-up or step-down, which makes good choice for applications requiring both. The single active switch is sufficient at lower power levels below 50W and two active switches connected in parallel can used for application which are greater than 50W and less then 200W, where component stresses are modest and a half- or full-bridge type topology is not needed. This type of converter is commonly used in applications requiring both high efficiency and stability, by providing electrical isolation through the transformer.

2.2. principle of operation:

Includes two modes of operation.

(a) Mode 1: This mode is during the time duration when the switch is "ON".
(b) Mode 2: This mode is during the time duration when the switch is "OFF".

1. Mode 1: The switch is closed, and voltage at input is applied across the primary winding of the transformer. Primary current starts to flow. The equivalent circuit is as shown in Fig- 2.1. Due to dot polarity of transformer a voltage appears across the secondary winding and energy is transferred from primary to secondary. The current and voltage at the primary and secondary are related through the turn's ratio (N_3/N_2) of the transformer.

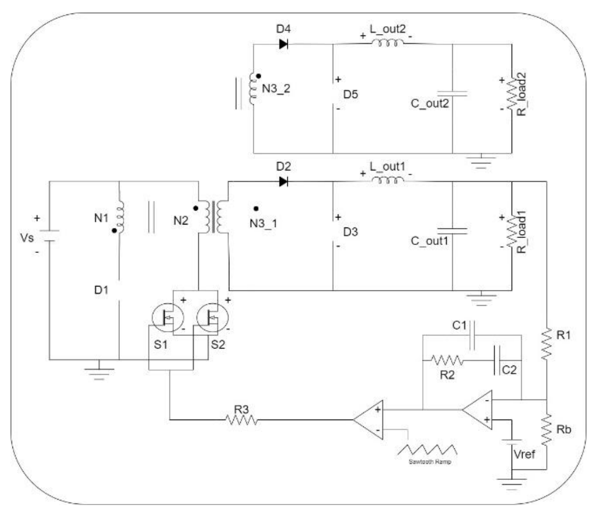

Fig-2.1 Forward converter equivalent circuit during mode 1.

As the switch is closed, the forward diode D_2 & D_4 becomes forward biased, and transformer secondary side voltage appears across a low pass filter constituted by L and C. The high frequency ripple is filtered by the low pass filter and output is delivered to the load. The freewheeling diode D_3 & D_5 remains OFF as it's reverse biased by the positive voltage appearing across its cathode. This mode is the powering mode as the input power is transferred to the load. Because of the opposite dot polarity, diode D_1 is reverse biased and remains OFF.

2. Mode 2: It is freewheeling mode. This mode begins when the switch opens. The transformer current falls to zero. But the filter inductor at secondary side maintains a continuous current through load through the freewheeling diode D_3 & D_5. The forward diode D_2 & D_4 remains OFF during this state. Due to opposite dot polarity of reset and primary winding, diode D_1 conducts and the magnetizing current flows in reverse direction, thus resetting the core. The equivalent circuit is as shown in Fig-2.2.

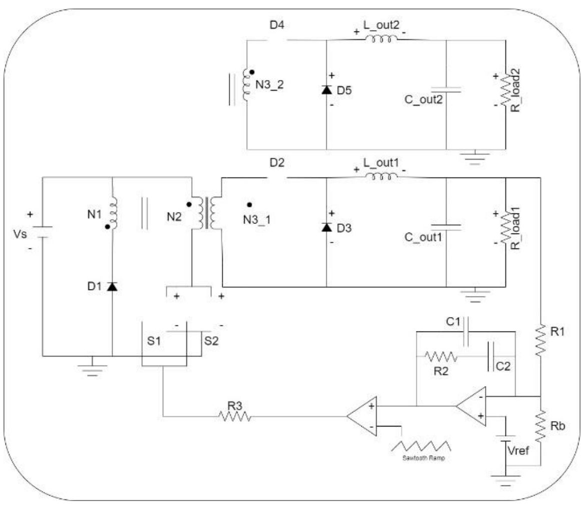

Fig-2.2 Forward converter equivalent circuit during mode 2.

3. SPECIFICATION AND DESIGN OF THE PROPOSED SYSTEM

3.1 Specification:

The design specification of the forward converter is represented in Table-1.

Table-1 Converter Specification

Parameter	Specification
Input Voltage	30V – 42V DC
Topology	Isolated Forward Converter
Output Voltage (Vout1 & Vout2)	5V
Output Current (Iout1 & Iout2)	8A
Switching Frequency	150KHz
Output Power	80W
Efficiency	>65%
Line Regulation	<1%
Load Regulation	<2%

3.2 Design equations:

Mode 1:
The equations governing the mode 1 are as follows:

Voltage across the primary winding N_p is given by,

$$V_p = V_{in} - V_Q \quad (3.1)$$

Voltage across the reset winding Nr is given by,

$$V_r = \frac{N_r}{N_p} V_{in} - V_Q \quad (3.2)$$

Voltage across the secondary winding Ns is given by,

$$V_s = \frac{N_s}{N_p} V_{in} - V_Q \quad (3.3)$$

Voltage at the cathode of Diode D_1 is given by,

$$V_b = \frac{N_s}{N_p}(V_{in} - V_Q) - V_{D1} \quad (3.4)$$

Voltage through output inductor is given by,

$$V_L = \frac{N_s}{N_p}(V_{in} - V_Q) - V_{D1} - V_{Out} \quad (3.5)$$

Current flowing through the output inductor increases and is given by,

$$I_L = \frac{\frac{N_s}{N_p}(V_{in} - V_Q) - V_{D1} - V_{Out}}{L} DT \quad (3.6)$$

Mode 2:
The equations governing the mode 2 are as follows:

Voltage through reset winding Nr is given by,

$$V_r = V_{in} + V_{D3} \quad (3.7)$$

Voltage through primary winding N_p is given by,

$$V_r = -\frac{N_r}{N_p}(V_{in} + V_{D3}) \quad (3.8)$$

Maximum voltage across the switch Q is given by the equation,

$$V_Q = (1 + \frac{N_p}{N_r})V_{inmax} \quad (3.9)$$

Voltage at secondary winding N_s is given by,

$$V_s = -\frac{N_s}{N_r}(V_{in} + V_{D3}) \quad (3.10)$$

Voltage across the output inductor is given by,

$$V_L = -V_{Out} - V_{D2} \quad (3.11)$$

Current through the output inductor decreases and is given by,

$$I_L = \frac{V_{D3} - V_{Out}}{L}(1-D)T \quad (3.12)$$

From Volt-Second balance adding equation 2.6 and 2.11 and equating it to zero, the output voltage is obtained as,

$$V_{Out} = \frac{N_s}{N_p}(V_{In} - V_Q)D - V_{D1} \quad (3.13)$$

Where,

V_{in} (V_s): Input voltage
N_p (N_2) : Number of turns in primary winding
N_r (N_1): Number of turns in reset winding
N_s (N_{3_1} & N_{3_2}) : Number of turns in the secondary winding
V_{D3} (V_{D1}) : drop Voltage across diode D_3
D : Duty ratio
T : Time period
V_{D1} (V_{D2} & V_{D4}) : drop Voltage across diode D_1
V_Q (V_{s1} & V_{s2}) : Voltage across switch Q
V_{out} (V_{out} & V_{out_1}) : Output voltage

4. EXPERIMENTAL RESULTS

4.1 simulation results:

To observe the performance of the converter developed, a simulation circuit is developed in the LT-spice as show in the Fig-3

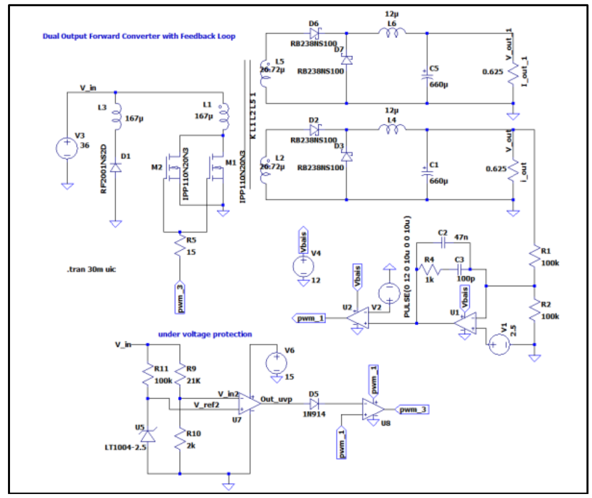

Fig-3 Forward converter simulation circuit

The simulation waveforms are shown in Fig-3.1, which includes output voltage and output current for both the outputs at nominal voltage (i.e. 36V).

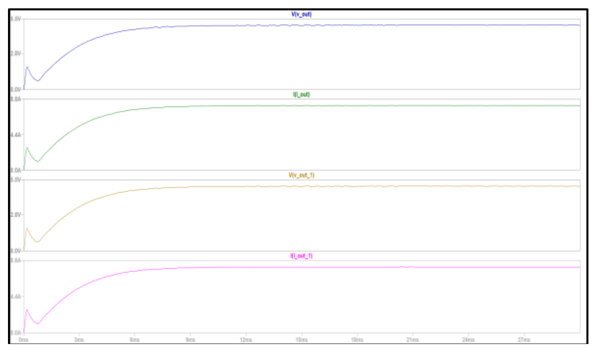

Fig-3.1 Forward converter output voltage & current for both the outputs

4.2 *Hardware results:*

Fig-4 shows the hardware experimental set-up for forward converter. The main components of set-up circuit are as follows:

- Power supply
- Digital CRO
- Forward dc-dc converter
- Electronic load

Fig-4 experimental set-up

The top view and bottom view of the forward converter as shown in Fig-4.1 & Fig-4.3 The main components of the forward converter in the hardware setup are as follows:

- EMI filter
- Main transformer
- MOSFET
- Bias inductor
- Secondary diodes
- Magnetic amplifier
- Output inductors
- PWM IC & Driver IC
- Output capacitors

Fig-4.1 converter top view

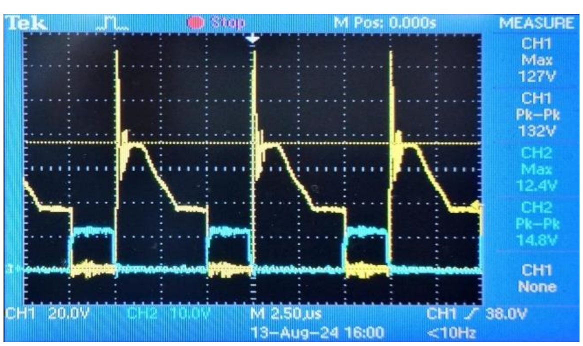

Fig-4.2 Gate and Drain Pulse

Fig-4.2 shows the gate and drain pulse of the MOSFET in the converter at the nominal voltage (i.e. 36V).

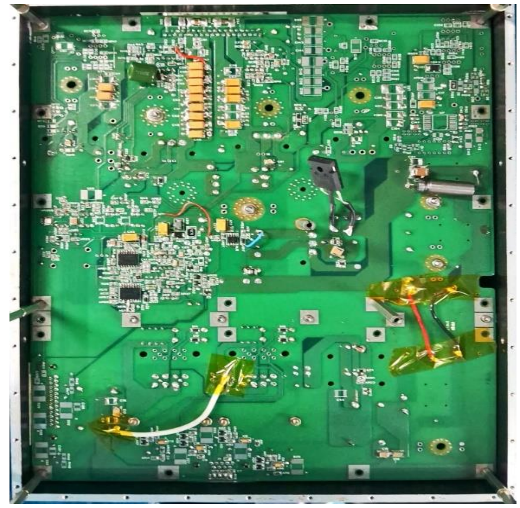

Fig-4.3 converter bottom view

Fig-4.4 shows the output voltage of the tested converter, (as both output are same i.e. 5V) for the nominal voltage (i.e. 36V).

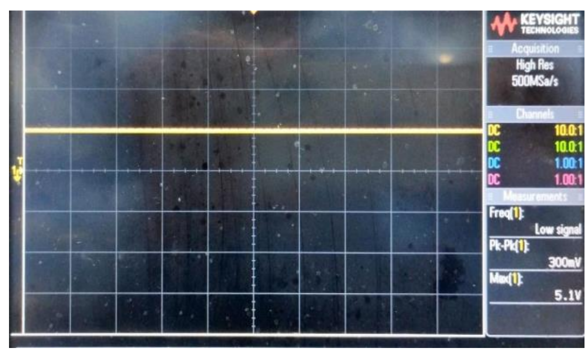

Fig-4.4 converter output voltage

Table-2 V_{DS}, V_{GS} & Duty cycle at different input condition

Input Voltage	Gate to Source Voltage (VGS)	Drain to Source Voltage (VDS)	Duty Cycle (D)	
			Calculated Value	Measured Value
30V	12V	118V	0.4	0.45
36V	12.4V	127V	0.33	0.37
42V	12V	140V	0.28	0.33

Table-3 output voltage at 100% load for different input condition and efficiency

Input Voltage (V)	100% load (Iout = 8A)					
	Iin (A)	Vout-1 (V)	Vout-2 (V)	Pin (W)	Pout (W)	Efficiency (%)
30	3.43	4.98	4.97	102.9	79.6	77.7
36	3.14	4.96	5.0	113.04	79.68	70.4
42	2.81	4.96	4.95	118.02	79.28	67.17

Table-2 shows the results of the gate and drain voltage for different input conditions with duty cycle that is been measured during the testing of the hardware. Whereas Table-3 show output voltage at 100% load condition and input current at different input voltage condition.

5. CONCLUSION

The hardware implementation and test results of the converter are presented. The analysis shows that the converter is operating at efficiency greater than 65% according to the specification. At maximum load conditions an efficiency of 67.17 % is achieved. Line regulation is less than 1%, load regulation and cross regulation less than 2% and thus meet the specifications. Gate, drain and output waveform for varies voltages are presented and analyzed. The experimental observations obtained under input and load conditions validate and justify the design to the proposed topology.

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