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Design and Optimization of Power-Efficient Non-Volatile SRAM Using Hybrid Architecture

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Abstract - *The demand for greater memory capacity in the electronics industry, coupled with the limitations of existing memory technologies due to scaling challenges, has driven the exploration of next-generation memory solutions. Technology scaling often leads to reduced stability, increased leakage currents, and higher standby power dissipation in electronic circuits. To address these issues, spin-transfer torque random access memory (STT-RAM) emerges as a promising alternative, offering features such as non-volatility, zero standby leakage, rapid access times, high density, efficient read and write performance, and low power usage. This study introduces a non-volatile hybrid 6T-4MTJ SRAM bit cell utilizing 32-nanometer technology. It is benchmarked against a conventional 6T SRAM bit cell to analyse the impact of process, voltage, and temperature (PVT) variations on key design metrics. The proposed hybrid 6T-4MTJ bit cell demonstrates reduced write delay spread and significantly lower leakage power compared to standard CMOS-based SRAM cells. Additionally, the MTJ-based SRAM design enhances overall stability by 19.49% while achieving a remarkable 92% reduction in power consumption.*

Key Words: **Magnetic Tunnel Junction (MTJ), MRAM, Spintronics, Non-volatile.**

1.INTRODUCTION

In 2023, the global Internet of Things (IoT) market generated $293.2 billion in revenue, a figure projected to triple to $621.6 billion by 2030. Among the critical components driving modern IoT-based technologies is electronic memory. Memory serves as a fundamental unit for storing data, including the instructions required for processing it. Memory is broadly categorized into two types: Random Access Memory (RAM) and Read-Only Memory (ROM). RAM is volatile, meaning it loses all stored data when the power supply is interrupted or switched off. In contrast, ROM is non-volatile and retains its data even in the absence of a power supply. This distinction makes memory an essential element in powering IoT applications efficiently and reliably.

Technologies such as CMOS (Complementary Metal Oxide Semiconductor), CNTFET (Carbon Nano Tube Field Effect Transistor), and FinFET (Fin-type Field Effect Transistor) play vital roles in enabling efficient data storage in memory. CMOS technology, widely used in designing integrated circuits, combines complementary NMOS and PMOS semiconductors in MOSFETs to create a variety of logic gates. This technology offers several advantages over alternatives like TTL, RTL, and NMOS, including a high noise margin, low static power dissipation, fast switching speed, and thermal efficiency. However, despite these strengths, CMOS devices exhibit slower read and write operations due to the relatively slow switching speed of their MOSFET components.

In advanced integrated circuit (IC) designs at 32nm or smaller, CMOS technology has faced limitations such as increased power consumption and leakage current. To address these challenges, emerging technologies like CNTFET and FinFET have gained traction. These technologies provide enhanced control over the thin silicon body, offering improved performance metrics. CNTFETs, for instance, simplify the manufacturing process by utilizing rolled-up hollow cylindrical carbon nanotubes. They also reduce source and drain width, leading to better gate capacitance, faster switching speeds, and improved short-channel immunity. Furthermore, CNTFETs require less power and propagation delay compared to CMOS devices.

However, CNTFETs have limitations, including a lower on-off current ratio compared to traditional transistors, which can make accurate data read and write operations more difficult. Additionally, defects in carbon nanotubes can alter their electrical properties, reducing the number of usable nanotubes in a device and potentially hindering the scalability of CNTFET-based circuits. These challenges can impact the reliability of CNTFETs in large-scale applications, particularly for critical operations like reading and writing data.

FinFETs feature a shorter channel length compared to CMOS transistors, enabling faster switching speeds and enhanced performance. Their larger effective channel width also supports higher drive currents, contributing to superior overall efficiency. However, the 3D architecture of FinFETs can increase the capacitance between the gate and the channel, potentially reducing the efficiency of read and write operations. This higher capacitance may also lead to slower switching speeds and increased power consumption. Additionally, compared to traditional CMOS transistors, FinFETs come with higher manufacturing costs due to their greater structural complexity and

variability, which can make production processes more challenging.

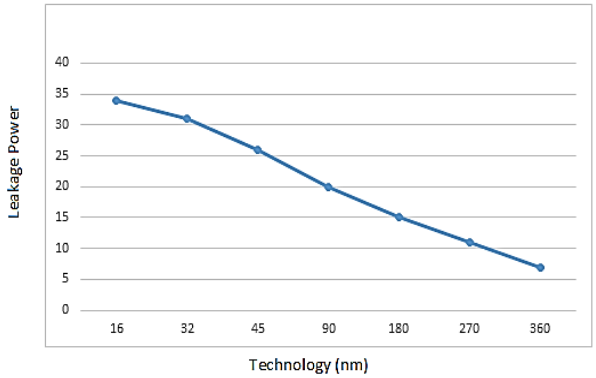

Chart -1: Leakage Power Analysis

As nanoscale technology continues to scale down, leakage power increases significantly (as illustrated in Chart-1), posing a major challenge due to the resulting higher power dissipation in electronic circuits. This makes further miniaturization of technology a complex and critical obstacle to overcome [4].

Spintronics, or spin electronics, is a field of study that explores the electron's intrinsic spin and magnetic moment alongside its electrical charge in solid-state devices. This technology leverages the spin property of electrons, in addition to their charge, to enable functionality. The spin property, which refers to the intrinsic angular momentum of elementary particles like electrons, neutrons, protons, and neutrinos, plays a central role in spintronics. Compared to traditional semiconductor devices, spintronic devices offer distinct advantages, such as non-volatility, greater scalability, and enhanced flexibility. The advancement of spintronics has been largely driven by the development of Magnetic Tunnel Junction (MTJ) technology [5].

A Magnetic Tunnel Junction (MTJ) consists of two ferromagnetic layers, typically made of magnetic metals like cobalt-iron, separated by a thin insulating oxide layer, such as magnesium oxide or aluminum oxide, with a thickness of approximately 1 nm. This ultra-thin insulating layer allows electrons to tunnel through the barrier when a bias voltage is applied across the two metal electrodes [6]. The tunneling current in MTJs is determined by the relative orientation of the magnetizations of the two ferromagnetic layers, which can be altered by an external magnetic field. MTJs offer several advantages, including excellent scalability, low power consumption, high-speed read and write operations, unlimited programming endurance, and enhanced scalability [7].

The tunnel magnetic resistance (TMR) ratio is defined as the ratio of the two resistances in a Magnetic Tunnel Junction (MTJ). Efforts are being made to improve the TMR ratio of MTJs to enable better integration with other devices. For hybrid circuits, a TMR in the range of 50% to 200% is typically sufficient to differentiate the voltage levels corresponding to logic states "0" and "1." This capability makes MTJs versatile for various applications [8][9].

$$TMR=\frac{RAP-RP}{RP}$$

Binary bits in magnetic memory based on Magnetic Tunnel Junctions (MTJs) can be stored in two distinct modes: Antiparallel (AP) and Parallel (P), as illustrated in Fig-1.

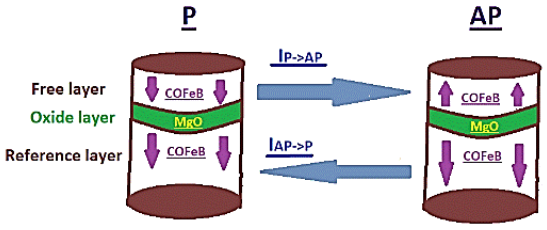

Fig -1: Magnetic Tunnel Junction

MTJs consist of layers with spinning electrons, where the direction of electron spin—either clockwise or counterclockwise—determines whether the device is in a Parallel or Antiparallel state. In these devices, one layer's orientation is fixed as a reference, while the orientation of the other layer can be changed depending on the applied voltage.

When the orientations of the two layers are opposite, a transition from parallel to antiparallel orientation occurs. Conversely, if the orientations are not opposed, a switch from antiparallel to parallel orientation is possible. The symmetry of the MTJ—whether parallel or perpendicular—depends on the materials used in its construction. Additionally, the insulating material on the drain side of the MTJ has a high melting point, which is crucial due to the significant power dissipation involved with the transistor connected to the MTJ's collector [10].

2. METHODOLOGY

2.1 1T-1MTJ

The "1T-1MTJ" structure, which includes one transistor and one magnetic tunnel junction with a tunneling oxide layer sandwiched between two ferromagnetic layers, is a widely used cell structure in Spin-Transfer Torque Magnetoresistive Random-Access Memory (STT-MRAM), as depicted in Fig. No. 3. In this structure, the "Reference layer" (RL) has a fixed magnetization, while the "Free layer" (FL) can have one of two potential magnetization orientations to represent binary data. [11]

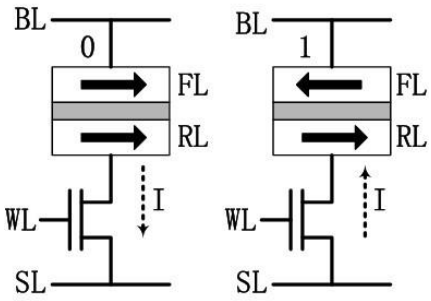

Fig -2: 1T-1MTJ design (a) bit '0' & (b) bit '1' operation

To write data to a Magnetic Tunnel Junction (MTJ), a current is passed through the transistor, generating a magnetic field that alters the magnetization orientation of the free layer. The stored data's state is determined by the direction of this magnetization. To read the data, a small voltage is applied across the MTJ, and the resulting resistance is measured. This resistance is dependent on the magnetization's orientation in the free layer and can be used to determine the stored data's state [11]

Write Operation: To write data to an MTJ cell, currents flowing in opposite directions are used to set the cell to a "0" or "1" state.

Writing "0": The MTJ is set to a parallel state, with the word line (WL) and bit line (BL) connected to the supply voltage (VDD), and the source line (SL) grounded, as shown in Figure No. 3(a). The transistor can operate in either the saturation or linear region, depending on its width.

Writing "1": The MTJ is set to an anti-parallel state, with the word line (WL) and source line (SL) connected to VDD, and the bit line (BL) grounded, as illustrated in Figure No. 3(b). In this case, the transistor operates in its saturation region.

Read Operation: There are two methods to read data from the cell: parallel (P) direction and anti-parallel (AP) direction.

Parallel Reading (P)**:** A very low voltage is applied between the bit line (BL) and source line (SL) during parallel reading. Once the word line (WL) is activated, current flows from the bit line (BL) to the source line (SL).

Anti-Parallel Reading (AP): During anti-parallel reading, the polarity of the voltage applied to the bit line (BL) and source line (SL) is reversed. As a result, current flows from SL to BL in the opposite direction.

2.1 Proposed 6T-4MTJ

Fig -3 illustrates the schematic design of the proposed 6T-4MTJ Hybrid SRAM bit cell, which mirrors the structure of a conventional 6T-SRAM cell. The cell employs cross-coupled CMOS inverters (latch) to store the complementary electrical states (Q, $\bar{Q}$) of volatile data. Beyond the CMOS latch, the design incorporates two non-volatile MRAM states integrated into the pull-up and pull-down networks of the latch. Each MRAM state contains two perpendicular STT-MTJs, which must maintain opposing states to ensure proper cell operation [12].

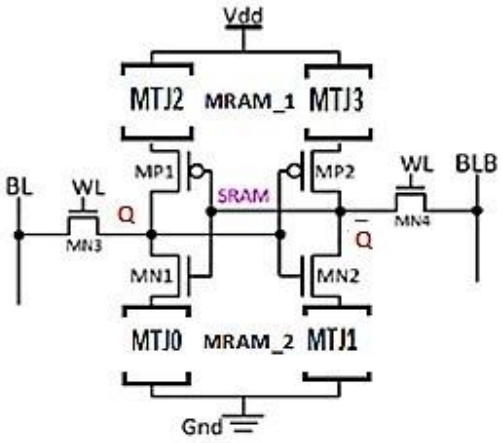

Fig -3: 6T-4MTJ

Write Operation:

To write data into a 6T-4MTJ circuit, a voltage pulse is applied to either Q or $\bar{Q}$, depending on the desired value. This pulse activates the transistor connected to the corresponding MTJ, enabling the connection of the bit line (BL) or its complement (BLB) to the selected MTJ, as determined by the state of Q or $\bar{Q}$. If the selected MTJ exhibits low resistance, the voltage on the bit line (BL) will remain relatively unchanged, indicating that the correct data value is already stored in the MTJ. Conversely, if the MTJ has high resistance, the voltage on the bit line (BL) will vary significantly, signaling the need to flip the magnetization of the MTJ to store the desired value.

To achieve this magnetization flip, a voltage pulse is applied to the complementary bit line (BLB or BL). This generates a magnetic field sufficient to alter the magnetization direction of one of the ferromagnetic layers within the MTJ stack. Known as "spin transfer torque," this process enables the magnetization direction to switch between parallel and anti-parallel states, effectively storing the new data value.

Read Operation:

Reading data from a 6T-4MTJ circuit involves applying a voltage to both Q and $\bar{Q}$, thereby activating the transistors linked to all MTJs. The resistance of each MTJ is then measured using the bit lines BL and BLB, with the stored data interpreted as 0 or 1 based on the resistance values.

If the selected MTJ has low resistance, the corresponding bit line voltage will show minimal change, indicating a stored value of 0. However, if the MTJ has high resistance, the bit line voltage will shift significantly, indicating a stored value of 1.

3. RESULTS AND DISCUSSIONS

3.1 1T-1MTJ

P to AP: Time-dependently, the MTJ's resistance rises to its maximum value, resulting in minimal current flow.

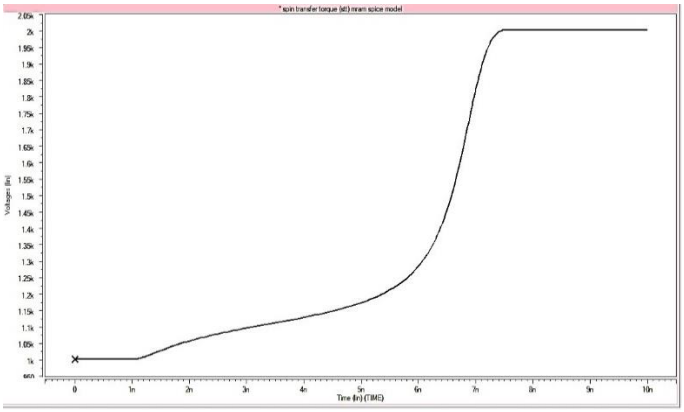

Fig -4: P to AP resistance analysis (Write 0)

AP to P: Time-dependently, 1T1MTJ's resistance is decreased to zero, allowing the maximum amount of current to flow through it.

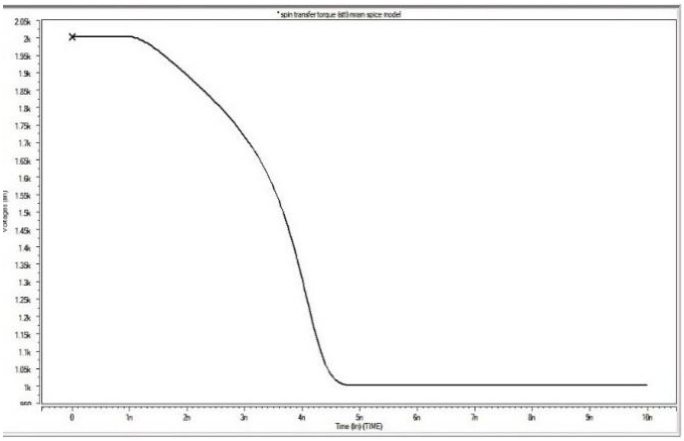

Fig -5: AP to P resistance analysis (Write 1)

3.2 1T-1MTJ: Proposed MTJ-based Non-Volatile Hybrid 6T-4MTJ SRAM bit cell

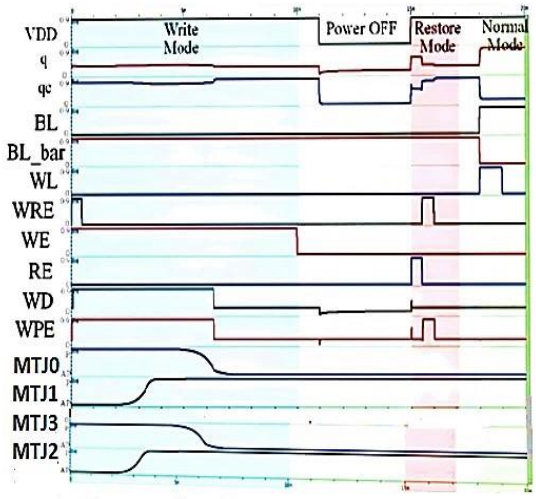

Fig -6: Simulation waveform of the proposed nonvolatile 6T-4MTJ SRAM bit cell

Write Operation for the Proposed 6T-4MTJ Cell**:**

The write operation for the proposed 6T-4MTJ cell is represented in the first region, highlighted in blue in Fig. No. 7. The initial states of MTJ1 and MTJ2 are assumed to be parallel, with MTJ1 starting in a low-resistance state (LRS) and MTJ2 in a high-resistance state (HRS). To store the values q = 0 and qc = 1, the states of both MTJs must be flipped.

During the entire write operation, the Write Enable (WE) signal remains active when set high. Additionally, the Write & Restore Enable (WRE) signal is pulsed with a duration of 1 ns to activate the transistor and initiate the write current. The voltage at the nodes q and qc determines the direction of the current flow through the MTJs.

The current flows from Vdd through MTJ2 and q, causing MTJ0 and MTJ3 to transition to a high-resistance state. Simultaneously, MTJ1 and MTJ2 are switched to a low-resistance state, successfully completing the write operation.[13]

3.3 1T-1MTJ: Overall Stability of Hybrid 6T-4MTJ SRAM bit cell

The static noise margin (SNM) is a measure of the stability of SRAM circuits. There are two primary methods for determining the SNM of an SRAM cell:

Graphical Method: This approach involves plotting the inverted characteristics of the SRAM cell and identifying

the largest square that can be enclosed between the mirrored curves.

Butterfly Curve Method: In this method, noise source voltages are applied to the nodes of the SRAM cell to generate a "butterfly curve" with two distinct lobes. The SNM is then calculated based on the largest square that can fit within these lobes.[14]

SNM Calculation:

The SNM is determined by finding the maximum side length of the square that fits within the butterfly curve's lobes. Mathematically, it is expressed as:

$$SNM = \frac{Maximum\ Length\ of\ square's\ diagonal}{\sqrt{2}}$$

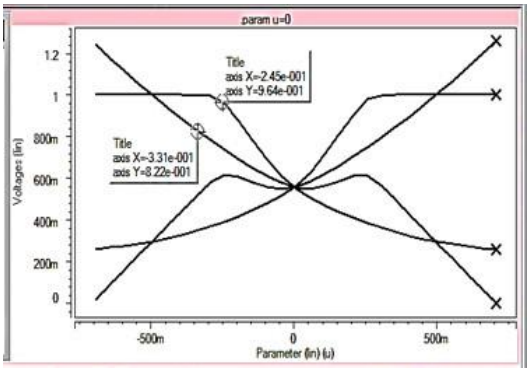

Fig -7: SNM curve of 6T-4MTJ MRAM cell

As a result, (Fig -7) shows that compared to the 6T SRAM bit cell, the overall stability has improved by 19.49%.

3.4 1T-1MTJ: Average power analysis of proposed 6T-4MTJ with standard 6T SRAM bit cell

Table No. 1 illustrates a comparison of the average power consumption of 6T and 6T-4MTJ circuits. It is observed that the 6T circuit consumes significantly more power. Incorporating MTJs into the circuit substantially reduces the average power consumption. Based on the recorded data, it is estimated that the addition of MTJs can decrease the average power consumption by approximately 92%.

Table -1: Average power comparison between 6T and 6T-4MTJ

Technology	Average Power (for 2.2 Volts)	
	6T	*6T-4MTJ*
32nm	1.38x10^-3	1.48x10^-4
45nm	3.68x10^-8	3.91x10^-9
90nm	5.95x10^-8	6.03x10^-9
180nm	5.19x10^-9	5.83x10^-10
270nm	6.23x10^-9	6.93x10^-10
360nm	8.83x10^-9	8.97x10^-10

3.5 Analysis of Write Access Time and Read Access Time Delays

Read Access Time or Read Delay

The read delay is defined as the time interval from the activation of the word line to the moment the output node transitions- either rising for a "1" read or falling for a "0" read. The 6T-4MTJ cell improves the switching time of the read operation, as it eliminates the need for additional voltage to initiate the cell, resulting in faster performance (Fig -7).

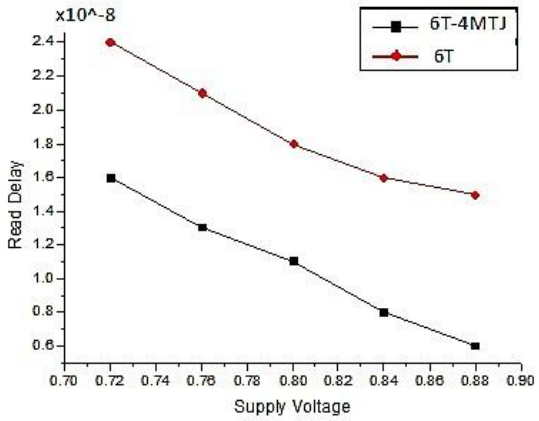

Fig -7: Read Delay Comparison

Write Access Time or Read Delay

The write delay is defined as the time interval from the activation of the word line to the point when new data is written to the bit cell nodes. The difference in write delay between the 10T (6T-4MTJ) and conventional 6T SRAM bit cells is negligible, as the dimensions of the pull-up and access devices, which primarily dictate the write delay, remain identical in both configurations. However, the 6T-4MTJ cell enhances the write operation speed due to its switching time, as it eliminates the need for an additional voltage to activate the cell (Fig. No. 10).

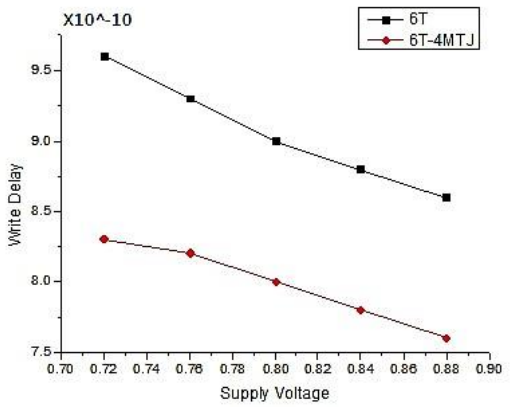

Fig -8: Write Delay Comparison

3. CONCLUSION

This study presents the design and analysis of a non-volatile hybrid 10T (6T-4MTJ) SRAM bit cell based on MTJ technology. The proposed cell is simulated using the HSPICE circuit simulator, followed by a comparative analysis with a conventional 6T SRAM bit cell. According to our findings, the MTJ-based SRAM bit cell achieves a significant reduction in power consumption by 92% while enhancing overall stability by 19.49%. The 6T-4MTJ design demonstrates notable advantages, including faster read and write operations, improved stability, and low power consumption.

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