

# Design Optimization of Universal Shift Registers: CMOS/FinFET vs. QCA

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**Abstract** - Quantum-dot Cellular Automata (QCA) is the new area of nanotechnology that gives an alternative paradigm of designing digital-circuitry thus it could replace the existing technologies, like CMOS and FinFET. Traditional semiconductor systems are faced with mounting problems, such as high-power dissipation, strong short-circuit effects and a lack of smaller size scaling. QCA is a better solution because of its high speed, low power consumption and capability of high density. QCA is an implementer of logical functions based on the spatial arrangement of electrons trapped in quantum dots instead of current flow, potentially a contender in nanoscale computing in the future. The current paper assesses various studies related to design and synthesis of Universal Shift Registers (USR) being executed by QCA Designer tool. USRs are essential parts of digital systems which give a mechanism of data storage, transfer and control. This paper has reviewed several different USR architectures based on QCA and has explored ways of improving their performance in terms of power consumption, runtime speed, and physical size. In addition, it compares QCA implementations with those similar designs based on CMOS and FinFET technology to identify the different benefits and restrictions of these technologies. Progressing findings show that QCA designs are faster, more energy efficient; however, they still face the pitfalls of fabrication related inefficiencies, complexities in clock distribution as well as noise susceptibility. It ends the study with both research directions to be further pursued by the application of potential solutions, and hypothesizes that with a further development of the methods of fabrication and testing, QCA could become a practical architecture of future nanoelectronics circuitry.

**Key Words:** CMOS, FinFET, QCA, Nanotechnology, Quantum Physics

## 1.INTRODUCTION

Constant scaling of the complementary metal-oxide-semiconductor (CMOS) technology has come close to a point where it is increasingly becoming impossible to reduce the size of the device. Leakage current, short-circuit effects, high power density and reduced reliability of the devices presently present a strenuous constraint on increased CMOS and FinFET devices performance. As a result, there exists a growing empirical research on the development of alternative nanotechnologies that can overlay physical and operational limits of traditional transistor based

architectures. An alternative is Quantum -Dot Cellular Automata (QCA). Unlike CMOS, which uses current flow and voltage switching, which is performed by transistors, QCA uses the positional order of electrons in nanoscale quantum dots to encode binary information. One example of an actual QCA cell is a four-quantum-dots system filled with two electrons; Coulombic repulsion causes the pair of electrons to be in two energy stable diagonal states, which are logic states 0 and 1. The propagation of information is based on electrostatic interaction between neighboring cells, but not on charge transport, which provides QCA systems with superior degrees of compactness, extremely low power consumption, and the possibility of extremely high operating frequencies. The following features of QCA make it an attractive propositional candidate to the implementation of future nanoscale digital systems, in particular to sequential logic elements, including latches, flip-flops, counters, and shift registers. In this regard, the Universal Shift Register (USR) is an essential element that is greatly used in data transfer, communication systems, and memory access. Traditional CMOS-based shift registers have a high number of transistors and consume high amounts of power, but QCA-based shift registers have few logic cells, a reduced physical area, and a better performance with less power. Researchers can design, analyse and optimise QCA circuits with design and simulation tools like the QCADesigner. This four-stage clocking scheme is unique to QCA that dictates electron tunneling and guarantees an orderly data flow that is essential to the dependable synchronous functioning of sequential circuits as well as the USR. Despite the current issues of QCA technologies in terms of the accuracy of their fabrication technique, thermal stability, and scalability of high fabrication rates, there is now a significant literature showing that QCA-based sequential circuits run faster, are smaller, and use less energy than CMOS or FinFET-based devices. These results demonstrate that QCA can become a very promising technology of next generation nanoelectronic systems. The current project is focused at the design and optimization of a Universal Shift Register that is implemented with QCA technology with a systematic comparison between its work and benefits against CMOS/FinFET implementation which ensures the possibilities of QCA as enhancing high-speed low-power future computing architecture.

## 2. LITERATURE REVIEW

a) Mistri et al. (2017) TG vs. GDI USR. Mistri et al. make comparisons of 4-bit USR designs using TG logic and GDI logic. With GDP implementation, the number of transistors is reduced by 31.5% and area decreases by 29.2%, delay by 26.7% and power consumption by 26.7%. Even though using CMOS technology, the work proves that CMOS simplification of logic components increases system USR efficiency, which is also applicable directly to quantum-dot cellular automata.

b) Saranya et al. (2013) Low-Power TGMS Flip-Flop USR. Reworking the TGMS flip-flop Saranya et al. have used aimed at minimizing internal capacitance and clock load only nine transistors reducing internal capacitance and clock load. Their 4-bit unit-resolution scheme (USR) has a reduction in flip-flop power consumption of 2.177mW to 1.524mW and a matching reduction in the unit-resolution power of their scheme to 33.223mW to 25.14mW. This paper shows that a similar flip-flop architecture has a positive effect on the behavior of sequential circuits, which is especially interesting in the case of quantum-dot cellular automata (QCA) -based universal computing registers.

c) Joshi and Jangir (2019) BICMOS SISO and SIPO Registers. The authors developed BICMOS based single-input-single-output (SISO) and single-input-multiple-output (SIPO) shift registers, which combine the energy efficiency of complementary metal-oxide semiconductor (CMOS) and the high-speed of bipolar junction transistors (BJTs). The resultant designs not only have lower propagation delays and a large reduction in power such as the SISO design running at on average 0.549mW or equivalent of 106  $\mu$ W power cut. In addition to this, the exploration also defines a principle of location-independent design by the discovery that the underlying flip-flop architecture could be improved and the result lead to an immediate performance gain relative to the performance of flip-flop shift-registers; and the notion can be generalized to quantum cellular automata (QCA).

d) Varun et al. (2025) TSPC+SVL for Low-Power Flip-Flops. The current design utilizes a 5T true single-phase clock (TSPC) flipflop coupled with a separated variable leakage (SVL) minimization strategy to both build variable leakage shift registers that are of significantly higher speed and lower power consumption. The power is reduced successfully to 1.630 to 0.44501171 mW and the propagation delay is very low and varies between 0.034 to 0.35ns. These results highlight the fact that improving clock architecture and reducing the number of transistors is an effective way to improve the performance of a sequential circuit, which is important in the design of QCA universal shift registers.

e) Pattanaik & Samal (2018) Pulse-Latch Based USR. Here, the authors replace traditional flip-flops with Static Sense Amplifier Shared Pulse Latches (SSASPL) and PTL-based

multiplexers to apply them in the creation of a 4-bit Universal Shift Register (USR) which is rather compact. This architectural change implies a 4-fold decrease in the number of transistors used in the design 216 92, a 532 ps propagation delay reduction to 324 ps, and a subsequent reduction in the dynamic power drawn. The suggested reduction in storage components and pulse-based functionality is consistent with the revolution of effective Quantum-dot Cellular Automata (QCA) design.

f) Sanadhya & Sharma (2025) Adiabatic Logic Shift Registers. The authors came up with a 4-bit Shift at the ultra-low-power architecture using DC-DB PFAL adiabatic logic. By as much as 85 per cent power is saved, and the PIPO register uses a dissipation of 0.026mW when a 45nm technology node is used. The concept of energy recovery and energy minimisation of switching can be compared to the clock gated, low energy consumption of quantum-dot cellular automata (QCA).

g) Isukapatla & Mala (2016) FinFET + SVL SISO Register. They designed a 5T TSET FinFET flip-flop using SVL to significantly decrease the amount of leakage that occurs during shift register operations. The total amount of power decreases significantly (CMOS: 1.486  $\mu$ W  $\rightarrow$  FinFET + SVL: 0.231  $\mu$ W). This study demonstrates that leakage should be minimized and that storage can also be simplified to improve efficiency, which parallels the reduction of switching energy in Quantum Cellular Automata (QCA).

h) Gurumurugan et al. (2017) FinFET + SVL for SISO/SIPO/PISO/PIPO. The authors applied Universal Single-Stage Voltage-Level Converter (U-SVL) and Low-Voltage Level Shifter (L-SVL) power gating to FinFET-based TSET flip-flops in order to reduce standby leakage in all types of shift-registers, with the SISO type exhibiting the lowest overall power consumption compared to its CMOS counterparts. The fundamental principle behind this approach is to eliminate unnecessary leakage and transitions—a concept that will be important when optimizing the functionality of a Universal Shift Register (USR) in QCA.

i) Hajare (2022) MOSFET vs FinFET Datapath Circuits. Hajare assesses MOSFET and FinFET data path circuitry at various technology levels, and concludes that FinFETs greatly outperform MOSFETs because of their significantly lower SCEs. FinFET-based designs have shown both decreased delay (as low as 8.93 ps) and have been able to run on nanowatts of power, while MOSFET designs failed before they were scaled down to 45nm. Therefore, the results support nanoscale design optimizations which are applicable to QCA USRs.

j) D'Aniello et al. (2025) SEU Effects in 16 nm FinFET Registers. The author's tested the Single Event Upset (SEU) behavior of a 150-bit FinFET shift register subjected to heavy-ion irradiation. The author's found that the SEU cross-

sections for the 150-bit shift registers were very low ( $\sim 10^{-9}$  cm<sup>2</sup>/bit), however the authors also found that the TMR was unable to mitigate errors resulting from multiple bit upset events created by the tight device spacing in the dense nanoscale designs used in this experiment. Therefore, the authors' findings demonstrate that dense nanoscale designs will be required to implement new forms of error mitigation; an area directly related to the high-density nature of many QCA circuit implementations.

k) Karthika and Krishnaveni (2023) QCA-Based Universal Shift Register Using Majority Logic and D Flip-Flops. In response to CMOS technology limitations, Karthika and Krishnaveni developed a 4-Bit Full Adder and Universal Shift Register (USR) based on Quantum-Dot Cellular Automata (QCA). A QCA-based USR that utilizes Majority Gates, Inverters and a QCA D-Flip-Flop along with four-to-one multiplexers supports left/right shifts, "hold" and "parallel load". Simulations in QCADesigner confirm that logic is correctly performed, that polarization of the cells is stable and that there is zone synchronized clocking. Compared to traditional CMOS implementations, the authors report that their design uses less area, has lower latency and consumes nearly zero power. The authors also address QCA implementation layout issues and describe an automated layout tool for developing large-scale QCA circuits.

l) Padma Selvi & Shyni (2017) QCA-Based Frequency Divider Design Using T, D, and JK Flip-Flops. Padma Selvi and Shyni (2017) introduce frequency dividers based on QCA, which are constructed with T, D, and JK flip-flops, and overcome CMOS drawbacks, such as leakage and scaling. The majority logic and model layouts are developed in QCADesigner to develop each flip-flop. The proper functioning of the dividing by two is checked, and T flip-flop has the minimal area (102 cells, 0.12  $\mu\text{m}^2$ ). The experiment shows that the complexity of flip-flops has a direct influence on the QCA area and the number of cells. Although it focuses on dividers, the work provides useful information on the design of QCA flip-flops, clocking, and sequential behavior, which is needed in the design of QCA-based Universal Shift Registers.

m) Nagul (2021) Design and Simulation of a QCA Nano-Calculator for High-Speed Arithmetic Operations. Nagul (2021) implements a nano-calculator with QCA, demonstrating that QCA is a promising post-CMOS technology, as it has a very low power consumption, small size, and a high speed. The paper describes the basics of QCA including cell structure, majority gates, cross-overs of wires, and four-phase clocking, and then applies arithmetic units such as adders, subtractors, multipliers, and dividers. Simulation using QCADesigner to verify correct functioning and stable propagation of clock zones. Though focused on combinational logic, the work provides important insights into QCA design, clocking, and layout techniques relevant for building your QCA-based Universal Shift Register.

n) Chakrabarty and Khan (2013) suggest an optimized and fault-tolerant QCA inverter design with minimum number of cells. The authors reduce the traditional 11-cell inverter to a compact 3-cell version but improve reliability by extending it to a 5-cell structure with near-ideal polarization ( $\pm 0.994$ ). Increasing the number of interacting cells improves stability and lowers defect susceptibility, according to kink-energy analysis. The optimized inverter shows an optimized area, a better fault tolerance and a better polarization than conventional designs. This work is valuable for QCA sequential circuits—including QCA-based USRs—where robust inverters directly impact performance and layout density.

o) Jeon (2023) presents advanced multi-layer QCA shift registers for low-energy LFSR operations in cryptographic systems. The study looks for limitations in previous QCA SR designs consisting of heavy use of majority gates, complex wiring, and high amounts of energy dissipation. To solve this, the author introduces multi-layer SISO and PIPO SR using simple interaction-based D-latches, which improve the modularity and reduce the crossover overhead. QCADesigner/E simulations demonstrate more than 27% of area-time performance and as much as 65% of energy dissipation reduction. The work is useful for QCA-based USR design, and provides the scalable, low-energy and layout-efficient sequential structures that can be applied directly to your project.

### 3. DISCUSSION AND RESEARCH GAP

Across all of the reviewed papers on the topic of CMOS and FinFET, it is clear that traditional transistor-based technologies are hitting physical limits because of leakage, short-channel effects, high power density, and reduced reliability in nanoscale nodes. Even advanced solutions such as FinFETs exhibit sensitivity to radiation, increased multiple-bit upsets, and a lack of stability as device dimensions decrease.

On the other hand, QCA literature consistently shows advantages such as ultra-low power, high device density, compact layouts, faster operation, and efficient sequential building blocks (flip-flops, latches, multiplexers, shift registers, etc.). However, the QCA papers also highlight major challenges such as clocking complexity, wire crossovers, fault sensitivity, low level of design automation, energy dissipation in long wires, and scalability issues in older QCA shift register architectures.

Although several QCA works optimize individual components (inverters, flip-flops, shift registers, nano-arithmetic units, etc.), there is still no research that presents a fully optimized Universal Shift Register (USR) that is modular, energy-efficient, multi-mode (SISO/SIPO/PISO/PIPO), and directly comparable with modern CMOS/FinFET-based USRs.

Therefore, based on the existing literature, there is a clear research gap: there is no unified, optimized, and scalable QCA-based Universal Shift Register that not only outperforms CMOS/FinFET USRs but also overcomes QCA-specific challenges such as clock alignment issues, energy dissipation, and layout complexity.

#### 4. PROPOSED METHODOLOGY

Circuit Diagram of a Universal Shift Register in (Fig 1.1) designed in Circuit Lab shows a proper idea of building blocks to designed QCA Layout.

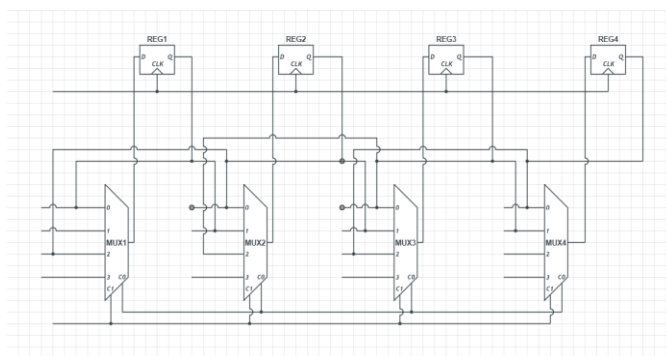


Fig -1: Universal Shift Register using 4:1 Mux and D-Flip Flop

In the above circuit diagram the basic building blocks of USR are given and it perform all 4 operations such as SISO, SIPO, PIPO, PISO (also known as shift and load operations). The S0 and S1 are control lines for the USR based on the logic behind these two control lines output takes place. The Flow dig. for the operation is also shown in Fig 1.2.

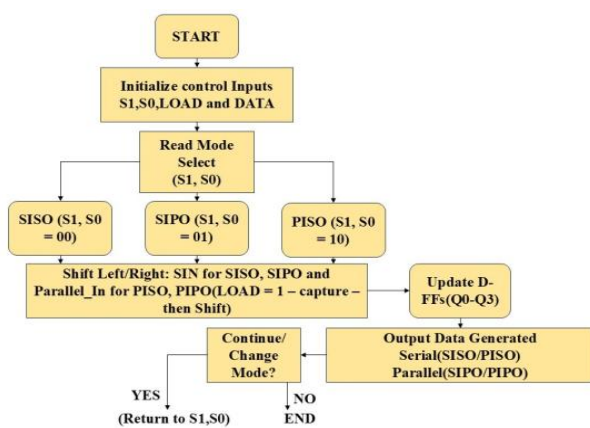


Fig -2: Flow Diagram for Universal Shift Register

The Universal Shift Register (USR) operates through four distinct modes determined by the control signals S1 and S0, allowing seamless switching between serial and parallel data transfers. The register begins by initializing key control inputs such as S1, S0, LOAD, and the serial and parallel data

lines, after which it remains idle until a specific operating mode is selected. Once the control lines are configured, the mode of operation is automatically identified: 00 enables Serial-In Serial-Out (SISO), 01 enables Serial-In Parallel-Out (SIPO), 10 enables Parallel-In Serial-Out (PISO), and 11 enables Parallel-In Parallel-Out (PIPO). This flexible mapping of control signals allows a single USR architecture to handle both gradual bit-by-bit shifting and full data transfers simultaneously, depending on application requirements.

During execution, the register performs data movement according to the selected mode. In SISO mode (00), each incoming serial bit propagates slowly through the flip-flop chain with every clock pulse until it reaches the output stage, ensuring both input and output remain strictly sequential. In SIPO mode (01), bits enter one after another via a single serial input but are stored internally across multiple flip-flops; once shifting is complete, the full set of values becomes instantly available on parallel output lines. Conversely, in PISO mode (10), the LOAD signal enables the full block of input data to enter the register simultaneously, after which LOAD is disabled and clock pulses begin shifting the stored bits outward one at a time through a single serial output. Finally, in PIPO mode (11), activating the LOAD signal places all input data directly into every flip-flop at once, and because shifting is unnecessary, the complete dataset appears immediately on the parallel output lines.

After any of the four operations, the flip-flop contents update according to the shifting or loading that has taken place, which determines whether the output emerges serially over time or parallelly all at once. The system then verifies whether another operation is required, and if so, it returns to mode-selection by adjusting S1 and S0. If no further shifting or loading is requested, the process halts. By dynamically reconfiguring behavior based on the control signals rather than hardware modification, the USR integrates SISO, SIPO, PISO, and PIPO capabilities within the same structural design. This makes it a highly versatile component in QCA-based systems, capable of supporting linear bitstream processing as well as simultaneous multi-bit transfers for efficient data handling.

#### 5. CONCLUSION

From the reviewed research papers related to the various results of the research papers on the different field of technology that are done by using the various types of transistors such as the Complementary Metal Oxide Semiconductor (CMOS), Fin Field Effect Transistor (FinFET) and the Quantum Cascaded Alloy (QCA) it is clear that the traditional transistor technologies are reaching the physical limit and the performance limit due to the scaling challenges, high leakage, power dissipation and reduced reliability. Even advanced nodes like 16nm FinFET have problems such as SEU vulnerability, increased layout density-induced faults and increased design complexity.

In general, Quantum-dot Cellular Automata (QCA) becomes a promising post-CMOS option due to its extremely small cell size, ultra-low power operation, high density and high speed switching based on electron polarization rather than current flow. Research on QCA flip-flops, multiplexers, inverters, multi-layer shift registers and nano-arithmetic circuits, shows reduced area, lower energy dissipation, easier routing and better performance compared to the designs of the same circuit in the field of CMOS/FinFET. However, QCA research also shows that there are difficulties like clocking synchronization, crossover design, layout sensitivity and a lack of strong large-scale automation tools.

Based on these findings, the objective of the present work is to design and implement an optimized Universal Shift Register (USR) with QCA technology taking advantage of:

- majority-logic primitives,
- low-energy QCA clocking,
- compact sequential elements,
- multi-layer and optimized routing strategies.

The goal is to have a USR which is smaller, faster and more energy-efficient than the corresponding counterparts using the more energy-efficient option, but also mitigate design limitations discovered in past QCA literature. This work is intended to make a contribution to scalable, low-power nanoscale sequential circuits that can be used for future high-density computing systems.

## REFERENCES

- [1] R. K. Mistri, R. Ranjan, P. Prasad, and A. Anupriya, "IC Layout Design of 4-bit Universal Shift Register using Electric VLSI Design System," *Int. J. Eng. Res. Technol.* (IJERT), vol. 6, no. 04, Apr. 2017, DOI: [10.17577/IJERTV6IS040320](https://doi.org/10.17577/IJERTV6IS040320).
- [2] M. Saranya, V. Vijayakumar, T. Ravi, and V. Kannan, "Design of Low-Power Universal Shift Register," *Int. J. Eng. Res. Technol.* (IJERT), vol. 2, no. 02, Feb. 2013, DOI: [10.17577/IJERTV2IS2551](https://doi.org/10.17577/IJERTV2IS2551).
- [3] N. Joshi and R. Jangir, "Low-Power, High-Speed SISO and SIPO Shift Registers using BiCMOS Logic," (2019).
- [4] Varun, S. et al., "True Single-Phase Clock (TSPC) Flip-Flop and Shift Register Designs — Comparative Study," (2025).
- [5] S. Pattanaik and S. Samal, "Design Alternatives for a 4-Bit Universal Shift Register Using Clock Pulse Sense Latch," (2018), DOI: [10.13140/RG.2.2.35366.96323](https://doi.org/10.13140/RG.2.2.35366.96323).
- [6] S. Sanadhya and S. Sharma, "DC-DB PFAL Adiabatic Logic for Low-Power Shift Registers," (2025).
- [7] K. Isukapatla and S. Mala, "FinFET-based TSET D Flip-Flop and SVL Techniques for Low-Power Shift Registers," (2016).
- [8] R. Gurumurugan et al., "FinFET Shift Registers with SVL Power-Gating for Leakage Reduction," (2017).
- [9] S. A. Hajare, "Performance Evaluation of Datapath Designs using MOSFET and FinFET Technologies," (2022).
- [10] F. D'Aniello, M. Tettamanti, S. A. A. Shah, and A. Baschiroto, "Single-Event Upset Characterization of a Shift Register in 16 nm Bulk FinFET Technology," *Electronics*, vol. 14, no. 7, 2025, DOI: [10.3390/electronics14071421](https://doi.org/10.3390/electronics14071421).
- [11] K. Karthika and M. Krishnaveni, "4-Bit Full Adder and Universal Shift Register Design using QCA," (2023).
- [12] J. Padma Selvi and P. Shyni, "Utilization of QCA Based Flip Flops to Design Frequency Dividers," *Int. J. Adv. Res. Trends Eng. Technol.*, vol. 4, Special Issue 10, Mar. 2017.
- [13] S. Nagul, "Quantum Dot Cellular Automata (QCA) — Nano Calculator," *Int. J. All Res. Educ. Sci. Methods*, vol. 9, no. 12, Dec. 2021.
- [14] R. Chakrabarty and A. Khan, "Design of a Fault-Free Inverter Circuit using Minimum Number of Cells & Related Kink Energy Calculation in QCA," in *Proc. Int. Conf. Computation and Communication Advancement (IC3A)*, Kalyani, India, 2013, pp. 369–373.
- [15] J.-C. Jeon, "Multi-Layer QCA Shift Registers and Wiring Structure for LFSR in Stream Cipher with Low Energy Dissipation in Quantum Nanotechnology," *Electronics*, vol. 12, Article 4093, 2023. DOI: [10.3390/electronics12174093](https://doi.org/10.3390/electronics12174093) (you can verify on publisher's site).