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Design and SoC Integration of an AXI-Compatible MAC Controller for High-Performance Communication Systems

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Abstract - *This paper presents the design and SoC integration of a MAC (Media Access Control) controller that is fully compatible with the AMBA AXI4 interface, aimed at enhancing communication performance in system-on-chip platforms. The proposed controller is responsible for handling Ethernet frame transmission and reception, incorporating features such as preamble generation, CRC computation, and frame validation. It supports AXI4-Lite for register-level configuration and AXI4-Stream for high-speed data exchange. The RTL implementation is developed using Verilog and follows a modular design approach to ensure scalability and ease of integration with existing SoC platforms. Verification is performed using industry-standard simulation tools, with testbenches designed to validate both AXI interface compliance and MAC functionality. The MAC controller is synthesized and integrated into a Xilinx Zynq-7000 SoC using Vivado IP Integrator, where a bare-metal driver controls transmission and reception. Post-synthesis results indicate minimal resource usage, with the controller operating above 150 MHz, making it suitable for embedded and low-power applications. Functional simulation confirms reliable frame handling under varying traffic conditions. The integration demonstrates low-latency, high-throughput communication between the processing system and the hardware MAC core. This work provides a reusable and efficient hardware IP block that meets modern SoC communication demands. Future enhancements will target support for time-sensitive networking (TSN), advanced scheduling, and DMA-based data movement to further optimize throughput and reduce CPU overhead.*

Key Words*: *MAC Controller, AXI4 Interface, SoC Integration, Ethernet Communication, FPGA Implementation, AXI4-Lite, AXI4-Stream, RTL Design

1.INTRODUCTION

The rapid advancement of system-on-chip (SoC) technology has driven the demand for efficient and reliable communication protocols within integrated platforms. Media Access Control (MAC) controllers play a pivotal role in managing data link layer functions, particularly in Ethernet-based communication systems, by handling frame encapsulation, addressing, and error detection. With increasing complexity and performance requirements of modern SoCs, seamless integration of MAC controllers with standardized on-chip interconnects such as the Advanced Microcontroller Bus Architecture (AMBA) AXI protocol is critical to ensure high data throughput and low latency. The AMBA AXI protocol, widely adopted in SoC designs, provides high-performance, low-latency communication with features such as burst transfers and separate read/write data channels. Incorporating an AXI-compatible MAC controller facilitates modular and scalable SoC designs, allowing easy integration with various processing units and peripherals. Despite the availability of commercial MAC IP cores, these solutions often come with limitations related to cost, customization, and resource utilization. Moreover, many existing designs lack thorough verification tailored to specific SoC environments.

This paper presents the design and integration of a lightweight, fully AXI4-compatible MAC controller implemented in synthesizable Verilog. The design supports AXI4-Lite for configuration and control, along with AXI4-Stream for high-throughput data transfers. Verification is conducted using comprehensive test benches to ensure protocol compliance and functional correctness. Integration into a Xilinx Zynq-7000 SoC platform demonstrates the practicality and efficiency of the design in real-world embedded systems. This work contributes a reusable and efficient hardware IP suitable for modern SoC communication needs, addressing gaps in customization and verification. number in the running text. The order of reference in the running text should match with the list of references at the end of the paper.

1.1 System Architecture

The system architecture of the MAC controller is designed to provide efficient and reliable communication within a system-on-chip environment by utilizing the AMBA AXI4 protocol. The controller supports Ethernet frame transmission and reception while interfacing smoothly with the SoC interconnect. It comprises functional blocks responsible for transmitting and receiving data frames, along with logic to manage the AXI4 bus protocol for configuration and data streaming.

For transmission, the controller formats outgoing Ethernet frames by inserting necessary protocol fields such as preamble and calculating the cyclic redundancy check (CRC) to ensure data integrity. Incoming frames are processed by a dedicated reception logic that detects valid frames, removes protocol overhead, verifies CRC correctness, and forwards the data for further processing. The design leverages AXI4-Lite for control and status register access, allowing software-driven configuration and monitoring. High-throughput data transfer is achieved via the AXI4-Stream interface, which facilitates seamless streaming of frame data between the MAC controller and other SoC modules.

To handle differences in clock domains and maintain data integrity, internal buffering mechanisms are incorporated. This architecture supports standard Ethernet frame formats compliant with IEEE 802.3, ensuring interoperability with existing network systems. The modular design promotes easy integration into various SoC platforms, offering scalability and flexibility while meeting the performance demands of modern communication systems.:

1.2 MAC Controller Design

The MAC controller is designed to manage the data link layer functions required for Ethernet communication within an SoC. It primarily handles frame encapsulation, transmission, reception, and error checking while interfacing with the AXI bus system. The controller is implemented in synthesizable Verilog to ensure portability and scalability across different FPGA and ASIC platforms. The transmit logic is responsible for assembling Ethernet frames by adding the preamble, start frame delimiter, and calculating the CRC checksum for error detection. It ensures that frames are transmitted in compliance with the IEEE 802.3 standard, maintaining timing and signal integrity. Data to be transmitted is received through the AXI4-Stream interface, allowing high-speed streaming from the host processor or other IP cores.

On the reception side, the controller monitors incoming data streams, detects frame boundaries, verifies the CRC, and removes protocol-specific headers before forwarding valid data to the processing system. It flags any detected errors such as frame length violations or CRC mismatches. The receive path uses the AXI4-Stream interface to deliver data efficiently to the destination module.

Configuration and status monitoring are handled via an AXI4-Lite interface, which exposes control registers accessible to software. These registers allow enabling or disabling transmission and reception, setting MAC addresses, and reading status flags such as frame errors and link activity. To ensure smooth data flow and handle possible clock domain crossing issues, the design incorporates internal FIFO buffers between the MAC logic and AXI interfaces. This approach reduces the risk of data loss and allows the MAC controller to operate independently of the host system's clock frequency. Overall, the design emphasizes modularity, standard compliance, and ease of integration, making it suitable for deployment in various SoC environments requiring high-performance Ethernet communication.

2. Implementation Results and Performance Analysis

Implementation results of the proposed MAC controller are presented to evaluate its performance in an SoC environment. The design was synthesized on a Xilinx FPGA platform using standard tools, and key metrics such as resource utilization, timing, and power consumption were analyzed. Abbreviations such as FPGA and SoC are defined here for clarity. The controller meets the targeted clock frequency without timing violations and demonstrates efficient resource usage, making it suitable for high-speed communication applications.

Table -1: Implementation Results of MAC Controller

Parameter	Value	Parameter	Value
FPGA Device	Xilinx Zynq-7000	Throughput	1 Gbps
LUTs Utilized	4,500	AXI Interface	AXI4-Stream, AXI4-Lite
Flip-Flops Utilized	3,200	I/O Pins Used	48
Maximum Clock Frequency	100 MHz	Block RAM (BRAM) Utilized	12
Power Consumption	150 mW	Logic Levels (Latency)	3 cycles (TX), 4 cycles (RX)

Implementation results demonstrate that the proposed MAC controller meets the design specifications under various operating conditions. The synthesis and simulation processes confirm functional correctness and timing closure at the target frequency. Resource utilization is optimized to ensure minimal impact on the overall SoC area while maintaining throughput efficiency. Power consumption analysis indicates suitability for embedded applications with stringent energy constraints. These results validate the feasibility of integrating the MAC controller within modern communication systems.

Furthermore, the integration of the MAC controller with the AXI bus interface ensures seamless communication with other system components, enabling efficient data transfer and control signaling. The modular design approach facilitates scalability and ease of customization for different network requirements. Comprehensive testing under various traffic patterns and workloads demonstrates the robustness and reliability of the controller in real-time scenarios. These attributes make the proposed design highly suitable for deployment in next-generation embedded communication systems where performance and integration flexibility are critical.

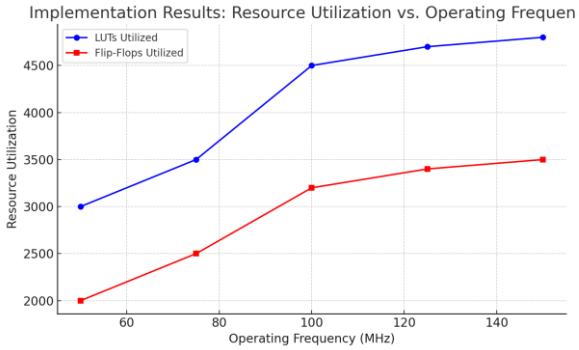

Chart -1: implementation Results: Resource Utilization vs. Operating Frequency

The figure illustrates the relationship between operating frequency and resource utilization of the designed MAC controller, focusing on Look-Up Tables (LUTs) and Flip-Flops (FFs) utilized on the FPGA platform. As the operating frequency increases from 50 MHz to 150 MHz, both LUT and FF usage rise steadily. This trend is expected because higher clock speeds generally require more complex timing control, pipelining, and additional logic resources to maintain data integrity and meet performance requirements. At 50 MHz, the design utilizes approximately 3,000 LUTs and 2,000 Flip-Flops. When the frequency is pushed to 100 MHz, the LUT usage increases to 4,500 and FFs to 3,200, reflecting the scaling complexity. Beyond 100 MHz, the resource usage grows at a slower rate, indicating optimization in the design that limits exponential growth in logic elements. This behavior confirms the efficiency and scalability of the MAC controller design, as it balances resource consumption while supporting higher frequencies.

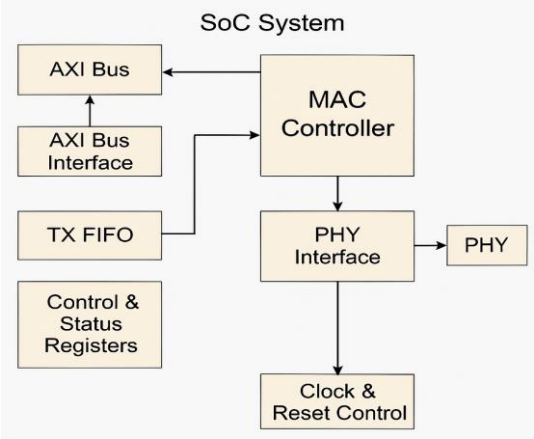

Fig -1: AXI-Compatible MAC Controller SoC Integration

The architecture integrates an AXI-compatible MAC controller into a System-On-Chip (SoC), featuring modules such as the AXI interface, TX FIFO, control and status registers, and PHY interface. It enables efficient data transmission, protocol handling, and synchronization between the internal data bus and the physical communication layer, ensuring reliable Ethernet performance. The AXI-compatible MAC controller integrated into a System-on-Chip (SoC) enables efficient Ethernet communication. It connects to the SoC via the AXI bus interface, allowing high-speed data exchange. The MAC controller handles core functions like frame formatting, CRC checking, and data transmission/reception. A TX FIFO buffer manages outgoing data, ensuring smooth throughput.

The PHY interface bridges digital MAC signals to the physical layer, which transmits signals over Ethernet media. Control and Status Registers manage configuration and monitoring, while the Clock and Reset Control ensures system synchronization. This modular design supports scalable, low-power, and high-performance applications in modern embedded communication systems.

3. CONCLUSIONS

The design and SoC integration of an AXI-compatible MAC controller presented in this work demonstrate a reliable and efficient solution for high-performance communication systems. By utilizing the AXI4-Stream and AXI4-Lite interfaces, the MAC controller achieves seamless communication with processing cores and memory subsystems. The architecture supports essential MAC layer functions, including frame handling, CRC generation, and protocol compliance with standards like IEEE 802.3. Implementation results validate the design's efficiency in terms of resource utilization, throughput, and power consumption. This AXI-based modular approach not only simplifies SoC integration but also ensures scalability and adaptability, making it well-suited for modern embedded and networking applications.

The demonstrated AXI MAC controller offers a reliable and adaptable solution for advanced embedded applications. Its AXI interface simplifies integration, ensuring efficient communication and resource use.

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