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RF POWER-BUDGET AND RECEIVER-NOISE CONSIDERATIONS FOR A TTD-BASED X-BAND QUAD T/R MODULE

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Abstract – *This article examines the RF performance considerations of a proposed four-channel true-time-delay transmit/receive module for X-band AESA radar. Its transmit chain includes a QPA0812 driver and CMPA851A01-series GaN power amplifier; the receiver chain incorporates a protective limiter, low-noise amplification and filtering. Keysight ADS is identified as the power-budget tool, while transmission-line and thermal studies support the RF design process. The nominal band is 9–10 GHz. The project reports gain above 25 dB, output power above 44 dBm and receiver noise figure below 3.5 dB per channel, although supporting numerical traces are not provided. The discussion distinguishes reported estimates from quantities that remain to be verified.*

Key Words: True time delay, Quad transmit/receive module, X-band, AESA radar, GaN, RF simulation.

1. INTRODUCTION

High-power transmission and low-noise reception impose different requirements on an AESA transmit/receive module. The transmit chain must deliver sufficient power without exceeding device limits, while the receiver must protect sensitive stages and minimize loss ahead of its first amplifier. TTD beam control adds a further requirement: signal timing should remain predictable as frequency changes. Insertion loss and amplitude variation must be included in the broader RF budget rather than evaluated in isolation. TTD beam control adds a further requirement: signal timing should remain predictable as frequency changes. Insertion loss and amplitude variation must be included in the broader RF budget rather than evaluated in isolation. Figure 1 shows the Switch configuration using the delay Line.

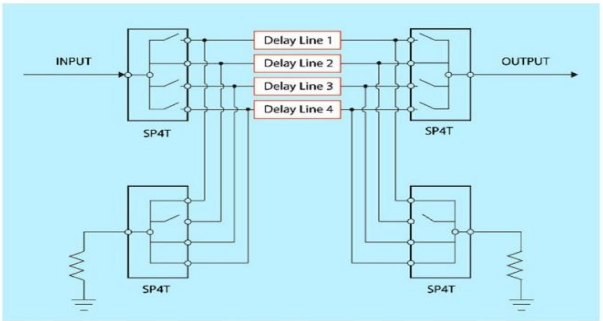


Fig -1: Architecture of the Switch configuration using the delay Line

2. DESIGN OBJECTIVES AND SYSTEM REQUIREMENTS

A 9–10 GHz operating range appears in the project abstract and simulation summary. Elsewhere, component descriptions and proposed tests refer to 8–10 GHz and 8.5–10.5 GHz. This paper therefore uses 9–10 GHz as its nominal design band, while retaining the broader ranges as items to clarify against the final specification.

3. PROPOSED QTRM ARCHITECTURE

Four RF channels share the overall module architecture, and each channel has separate transmit and receive signal paths. The beamforming section supplies programmable delay and gain settings. A circulator or comparable routing device, limiter, low-noise amplifier, filters, and bias/control circuits complete the signal chain. The available schematic details one RF channel; the project description indicates that this section is repeated for the other three. Figure 2 represents the QTRM architecture with power and digital section.

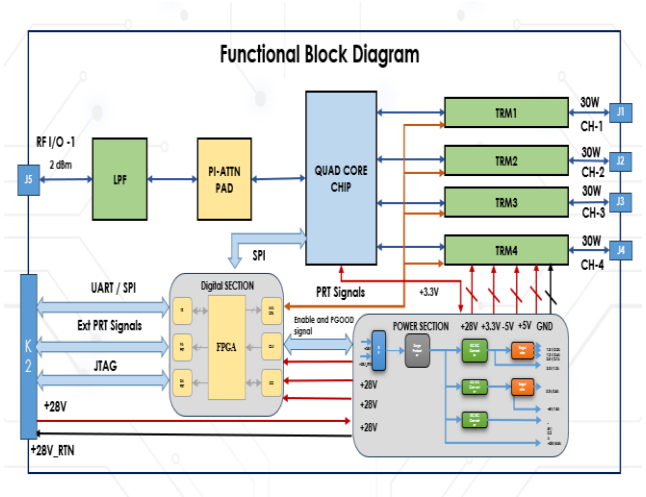


Fig -2: Architecture of the Quad-Transmit and Receive Module (QTRM).

3.1. Beamforming and Control Core

The design narrative names the ADAR4002 as its delay-and-gain-control device, whereas the bill of materials identifies an ADAR1000 four-channel beamformer. Because these selections imply different system arrangements, the final circuit drawing, simulation model, and procurement list need to be checked before a specific part can be confirmed. The neutral term "TTD/beamforming core" is used here until that discrepancy is resolved.

3.2. Transmit Chain

For transmission, the proposed signal path uses a QPA0812 driver ahead of a CMPA851A01-series GaN power amplifier. The first device supplies drive to the final RF stage. A realistic output-power estimate must account for the available gain, compression behavior, passive insertion losses, mismatch, and any deliberate operating back-off at each stage.

3.3. Receive Chain and Protection

On reception, the stated parts include a TGL2209 protective limiter and SAC4012BQ5 low-noise amplifier, together with filters and the beamforming section. The limiter helps prevent excessive incident power from reaching sensitive circuitry. Since attenuation before the first low-noise stage can substantially worsen the noise figure, the exact ordering and losses of the circulator, limiter, and filter must be established from the final schematic.

4. DESIGN AND SIMULATION METHODOLOGY

4.1. RF Chain Power Budgeting

A practical transmit budget must consider several key factors: the input drive, the gain of each amplifier, passive insertion losses, mismatch, and compression margin. For receiver assessments, it is essential to evaluate losses that occur before the first Low Noise Amplifier (LNA), the performance of limiters, as well as the cascaded gain and noise figure. These elements collectively influence overall system performance and efficiency.

4.2. Transmission Line and PCB Analysis

The board study focuses on using Rogers RO4003C material as an 8-mil dielectric reference along with coplanar waveguide with ground (CPWG) routing. Key electromagnetic checks must include assessments of 50-ohm line behavior, ground-return continuity, via fences, transmission line bends, component transitions, adjacent-channel coupling, and frequency-dependent loss. For the analysis to be repeatable, the published layout must detail substrate and copper thicknesses, dielectric properties, conductor width, CPWG spacing, and ground-via pitch. Figures 3 and 4 provide insights into the ADS schematic RF circuit design and analyze linear and nonlinear parameters, such as gain, output P1dB, TOI, output power, and SNR for each component.

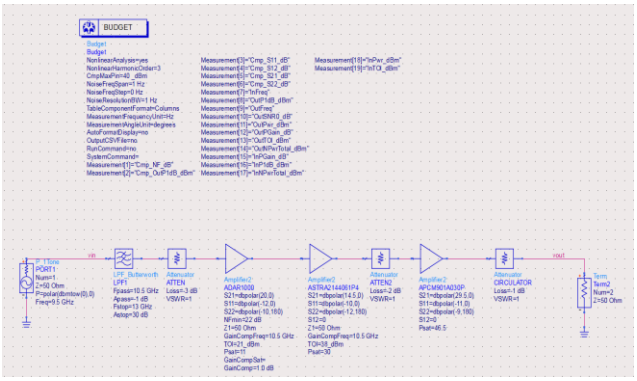


Fig -3: RF Circuit Design Budget Analysis in Keysight ADS

Cmp_Index	Cmp_RefDes	Cmp_S21_dB	...p_OutP1dB_dBm	Cmp_NF_dB
0	LPF1	-0.055	1000.000	0.000
1	ATTEN	-3.000	1000.000	3.000
2	ADAR1000	20.000	9.074	22.264
3	ASTRA2144061P4	14.500	27.195	0.000
4	ATTEN2	-2.000	1000.000	2.000
5	APCM901A030P	29.500	43.087	0.000
6	CIRCULATOR	-1.000	1000.000	1.000

Cmp_Index	InFreq	InPGain_dB	InP1dB_dBm	InTOI_dBm	InNPwrTotal_dBm	InPwr_dBm
0	9.500E9	-0.136	-14.875	-1.578	-173.855	-0.136
1	9.500E9	-0.136	-15.011	-1.578	-173.991	-0.136
2	9.500E9	-3.350	-18.225	-4.620	-174.223	-3.350
3	9.500E9	9.410	1.230	17.379	-133.273	9.410
4	9.500E9	23.443	15.860	31.813	-118.834	23.443
5	9.500E9	21.223	13.641	29.640	-121.054	21.223
6	9.500E9	45.987	1000.000	1000.000	-91.195	45.987

Cmp_Index	Cmp_RefDes	OutFreq	OutPGain_dB	OutP1dB_dBm	OutTOI_dBm	...wrTotal_dBm	OutSNR0_dB	OutPwr_dBm
0	LPF1	9.500E9	-0.136	1000.000	1000.000	-173.991	173.855	-0.136
1	ATTEN	9.500E9	-3.350	1000.000	1000.000	-174.223	170.873	-3.350
2	ADAR1000	9.500E9	9.410	7.335	21.000	-133.273	142.683	9.410
3	ASTRA2144...	9.500E9	23.443	20.992	32.325	-118.834	142.277	23.443
4	ATTEN2	9.500E9	21.223	18.772	29.873	-121.054	142.277	21.223
5	APCM901A03...	9.500E9	45.987	41.851	56.466	-91.195	137.181	45.987
6	CIRCULATOR	9.500E9	44.987	40.851	55.147	-92.195	137.181	44.987

Fig -4: Data Analysis for linear and non-linear parameters of RF Chain.

5. RESULT AND DISCUSSION

5.1. RF Performance Summary

The proposed design achieves a gain exceeding 25 dB and a transmit output of 44 dBm, with a receiver noise figure lower than 3.5 dB. However, to ensure reproducibility and facilitate comparison, it is essential to provide frequency-indexed results along with stage-level model information.

5.2. Layout and Thermal Observations

Although the project material presents layout and thermal simulations, it lacks numerical values for insertion loss, reflection, isolation, coupling, and thermal boundary conditions. Consequently, the current evidence does not substantiate any quantitative claims regarding improvements in compactness, RF isolation, or temperature performance. The primary outcome of the project is the integration and evaluation procedure proposed; however, numerical conclusions are contingent upon a review of the original simulation outputs.

5.3. EM Model PCB Layout Simulation

A TTD-centered design requires clear evidence of delay performance metrics, including delay settings, step size, maximum delay, and state-dependent insertion loss. Critical comparisons involving frequency and delay can be expressed through the relationship $\varphi(f) = -360° \, f \, \tau$. Claims about reduced beam squint should be verified through comparative phase-shifter steering analyses over the specified frequency range. The existing material provides a conceptual overview, yet lacks adequate delay-state data for meaningful comparisons. Additionally, Figures 5 and 6 illustrate the QTRM PCB layout analysis, with the latter indicating S-Parameter results exceeding 25dB.

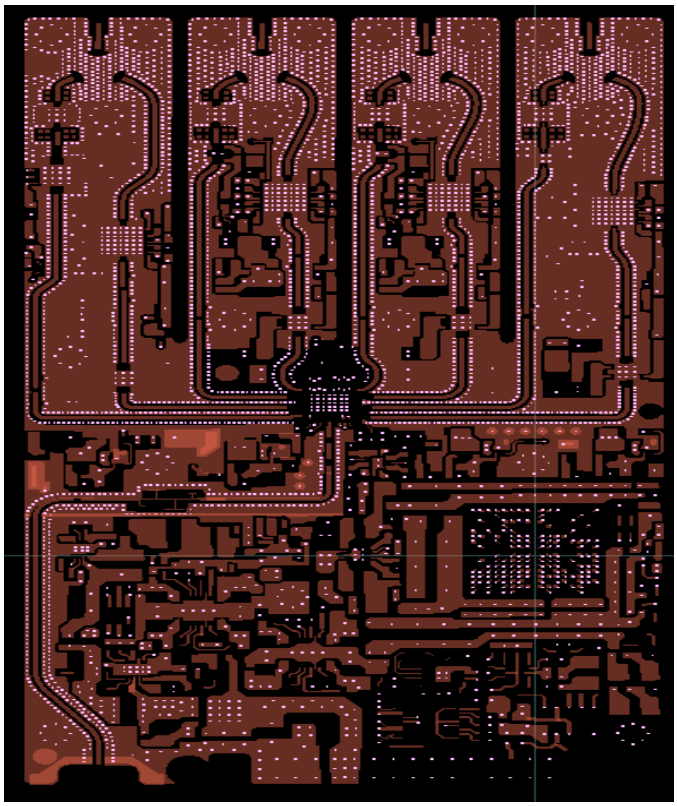


Fig -5: Layout Analysis of QTRM PCB in Keysight ADS

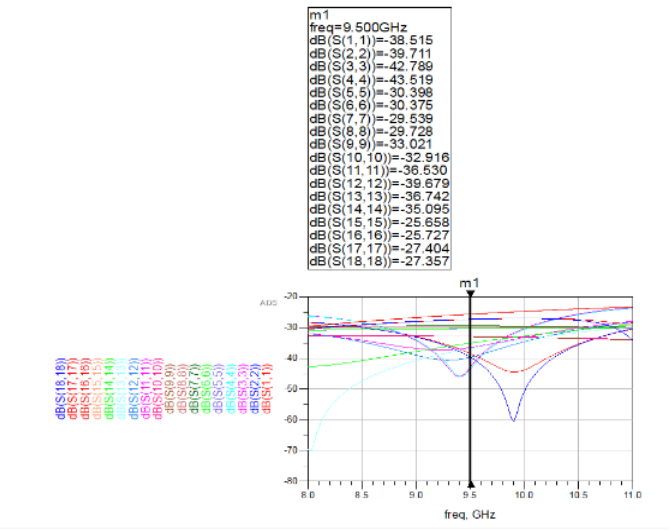


Fig -6: Simulated S-Parameter results of QTRM PCB Layout

6. CONCLUSION

The proposed RF-chain approach serves as a foundation for analyzing transmitter power and receiver sensitivity in a TTD-based QTRM. However, additional evidence is required to assess aspects such as delay-state behavior, frequency sweeps, thermal limits, and the consistency measured across channels.

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