A Study on Comparative Analysis of Multilevel Inverter for EV Applications

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Abstract - *Multilevel inverters (MLIs) play an important role in modern power electronic systems due to their ability to generate high-quality output voltage with reduced harmonic distortion. Among the different configurations, the three-level diode clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), and cascaded H-bridge multilevel inverter (CHBMLI) are widely used in various applications such as renewable energy systems and motor drives. This paper presents a comparative analysis of these three three-level multilevel inverter topologies using MATLAB/Simulink. The comparison is carried out based on total harmonic distortion (THD), which is a key parameter used to evaluate the quality of the output voltage waveform. Each inverter topology is modeled and simulated under similar operating conditions to ensure accurate performance comparison. The output voltage waveforms and harmonic spectra are analyzed using FFT analysis in MATLAB/Simulink. The simulation results demonstrate the differences in harmonic performance among the three inverter topologies. The study provides insights into selecting the most suitable three-level multilevel inverter topology for applications requiring improved power quality and reduced harmonic distortion.*

1. INTRODUCTION

Multilevel inverters (MLIs) have become an important technology in modern power electronic systems due to their ability to produce high-quality output voltage with reduced harmonic distortion. Conventional two-level inverters generate output voltages with large harmonic components, which may lead to increased switching losses, electromagnetic interference, and reduced efficiency in electrical systems. To overcome these limitations, multilevel inverter topologies have been developed to produce stepped voltage waveforms that closely approximate a sinusoidal waveform. Among the different multilevel inverter configurations, the diode clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), and cascaded H-bridge multilevel inverter (CHBMLI) are the most commonly used topologies. These inverters generate multiple voltage levels by using power semiconductor switches, capacitors, and DC voltage sources. By increasing the number of voltage levels, the output waveform quality improves and the harmonic distortion decreases significantly. In power electronic systems, harmonic distortion is a critical factor that affects the overall performance of electrical equipment. Excessive harmonics can cause additional power losses, overheating of devices, and poor power quality. Therefore, Total Harmonic Distortion (THD) is widely used as an important parameter to evaluate the performance of inverter topologies. This paper presents a comparative study of three-level multilevel inverter topologies, including diode clamped, flying capacitor, and cascaded H-bridge inverters. The comparison is carried out using MATLAB/Simulink simulation models. Each inverter is designed under similar operating conditions to ensure an accurate comparison. The performance of the inverters is analyzed based on the Total Harmonic Distortion (THD) of the output voltage waveform. The objective of this study is to analyze and compare the harmonic performance of these three inverter topologies and identify the most suitable configuration for applications requiring improved power quality and reduced harmonic distortion.

1.1 Literature Review

The advancement of multilevel inverter (MLI) technology has gained considerable interest in contemporary power electronics because of its capability to produce superior output voltage with lower harmonic distortion and enhanced overall power quality. Various research studies have investigated different multilevel inverter topologies and their performance characteristics, particularly focusing on Diode-Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI), and Cascaded H-Bridge Multilevel Inverter (CHBMLI).

A comparative study presented in [1] analyzes these three inverter configurations based on parameters such as circuit structure, number of switching devices, output voltage waveform, and harmonic distortion characteristics. The study explains that multilevel inverters produce stepped output voltage waveforms that closely approximate sinusoidal waveforms, thereby reducing harmonic components and improving the overall efficiency of the power system. The results also indicate that the cascaded H-bridge inverter provides better harmonic performance and modularity due to its independent DC sources and flexible configuration. Another study in [2] highlights the importance of Pulse Width Modulation (PWM) techniques in controlling the switching operations of inverter devices. PWM methods, particularly multicarrier PWM techniques, help reduce harmonic distortion and improve the quality of the output voltage waveform. The performance comparison of CHB, NPC, and FC inverter topologies under PWM control shows that the cascaded H-bridge inverter generally produces lower harmonic distortion and improved voltage waveform quality compared to the other topologies. A simulation-based investigation reported in [3] analyzes multilevel inverter topologies using MATLAB/Simulink, where diode-clamped, flying capacitor, and cascaded H-bridge inverters are modeled and evaluated in terms of output voltage waveform, switching behavior, and Total Harmonic Distortion (THD). The harmonic spectrum of the inverter output voltage is obtained using Fast Fourier Transform (FFT) analysis, demonstrating that multilevel inverters significantly reduce harmonic distortion compared to conventional inverters, while the cascaded H-bridge topology shows improved performance due to its modular structure and reduced switching losses.

Further analysis presented in [4] explains the structural and operational differences among multilevel inverter topologies. The diode-clamped inverter uses clamping diodes and DC-bus capacitors to generate multiple voltage levels, which makes it suitable for high-voltage applications but increases circuit complexity as the number of voltage levels increases. The flying capacitor inverter employs floating capacitors to produce intermediate voltage levels and offers advantages such as voltage balancing capability and redundant switching states, although it requires a large number of capacitors, increasing system cost and complexity. In contrast, the cascaded H-bridge inverter consists of multiple H-bridge cells connected in series, each supplied by separate DC sources, which provides a modular structure and scalability for higher voltage levels. Research focusing on harmonic performance in [5] analyzes how different multilevel inverter topologies influence harmonic distortion levels in the output voltage waveform. Harmonics in power systems can lead to additional power losses, overheating of electrical equipment, and reduced system efficiency. Therefore, minimizing harmonic distortion is an important objective in inverter design, and increasing the number of voltage levels significantly improves waveform quality.

Another study in [6] explains the use of FFT techniques to analyze harmonic components in inverter output waveforms. FFT converts time-domain signals into frequency-domain representations, allowing accurate identification of harmonic frequencies. The performance of multilevel inverters is commonly evaluated using Total Harmonic Distortion (THD), which measures the ratio of harmonic components to the fundamental component of the waveform.

A detailed review presented in [7] describes the operating principles of the diode-clamped inverter, also known as the Neutral Point Clamped (NPC) inverter, where the DC bus voltage is divided into multiple levels using capacitors and clamping diodes.This configuration reduces voltage stress on switching devices and improves waveform quality, although voltage balancing becomes challenging at higher levels. Another study in [8] investigates the simulation of the cascaded H-bridge multilevel inverter using MATLAB/Simulink and demonstrates that this topology produces stepped output voltage waveforms with lower harmonic distortion compared to conventional inverters. The modular structure of the cascaded H-bridge inverter enables easy expansion to higher voltage levels and makes it suitable for renewable energy integration, industrial power converters, and motor drives. Furthermore, research presented in [9] discusses the design and simulation of a three-level multilevel inverter for power electronic applications, where the results indicate improved output voltage waveform quality, reduced harmonic distortion, and lower switching stress on power devices. Overall, the reviewed literature indicates that multilevel inverter technology plays a significant role in improving power quality in modern power electronic systems. Among the different inverter configurations, the cascaded H-bridge multilevel inverter is often considered the most advantageous due to its modular structure, lower harmonic distortion, and flexibility in generating multiple voltage levels. These characteristics make multilevel inverters highly suitable for applications such as **renewable energy systems, motor drives,** electric vehicles, and high-power industrial power conversion systems.

2. MULTILEVEL INVERTER

A multilevel inverter (MLI) is a power electronic device that converts direct current (DC) into alternating current (AC) by producing multiple voltage levels at the output instead of just two levels as in conventional inverters. By generating several stepped voltage levels, the output waveform becomes closer to a sinusoidal waveform, which helps in reducing harmonic distortion and improving power quality. Multilevel inverters are widely used in medium- and high-power applications such as renewable energy systems, motor drives, electric vehicles, and industrial power converters because they offer advantages like lower switching losses, reduced electromagnetic interference, and improved efficiency. The main types of multilevel inverter topologies include diode-clamped (neutral point clamped), flying capacitor, and cascaded H-bridge inverters, each having different circuit structures and operational characteristics. Among these, the cascaded H-bridge inverter is often preferred due to its modular structure, lower harmonic distortion, and flexibility in generating multiple voltage levels. Overall, multilevel inverters play a crucial role in modern power electronic systems by providing high-quality AC output with reduced harmonics and enhanced system performance.

2.1 Diode Clamped multilevel inverter

Fig. 2.1 illustrates the basic structure of a three-level diode-clamped multilevel inverter, also known as a Neutral Point Clamped (NPC) inverter. In this configuration, the DC input voltage V_{dc} is divided into two equal voltage levels using two capacitors C_1 and C_2, which create a neutral midpoint in the circuit. The inverter leg consists of four switching devices S_1, S_2, S_3 and S_4, which control the generation of the output voltage supplied to the load. Additionally, clamping diodes D_1 and D_2 are used to connect the midpoint of the capacitors to the switching nodes, ensuring that the voltage across each switch is limited and properly balanced. By operating the switches in different combinations, the inverter can produce three distinct output voltage levels: $+V_{dc}/2$, 0, and $-V_{dc}/2$. These stepped voltage levels help generate an output waveform that closely resembles a sinusoidal waveform, thereby reducing harmonic distortion and improving power quality. Due to these advantages, the three-level diode-clamped inverter is widely used in medium- and high-power applications such as motor drives, renewable energy systems, and industrial power conversion systems.

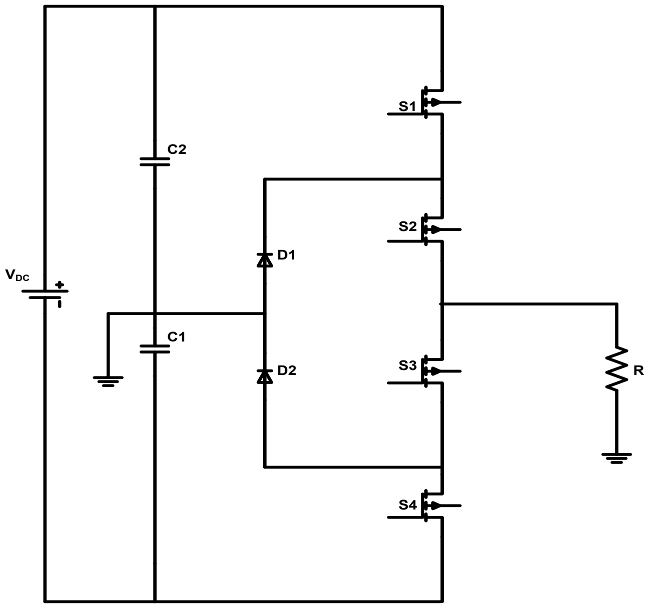

Fig -1: Diode Clamped Multilevel Inverter

2.2 Flying Capacitor Multilevel Inverter

Fig. 2.2 shows the circuit configuration of a three-level Flying Capacitor Multilevel Inverter (FCMLI). In this topology, the DC input voltage is converted into AC using multiple power semiconductor switches (S1, S2, S3, and S4) along with flying capacitors that help generate intermediate voltage levels. The flying capacitor is connected between the switching nodes and acts as an energy storage element that charges and discharges during switching operations. Unlike the diode-clamped inverter, this topology does not use clamping diodes; instead, it uses capacitors to maintain the required voltage levels. By controlling the switching states of the inverter switches, the circuit can generate three output voltage levels: +Vdc/2, 0, and −Vdc/2. The flying capacitor also helps maintain voltage balancing and provides multiple switching combinations to achieve the same output level, which improves the flexibility of control. Due to the stepped output waveform produced by this inverter, harmonic distortion is reduced and the output voltage becomes closer to a sinusoidal waveform, resulting in improved power quality. Therefore, the flying capacitor multilevel inverter is widely used in high-power applications such as motor drives and industrial power conversion systems.

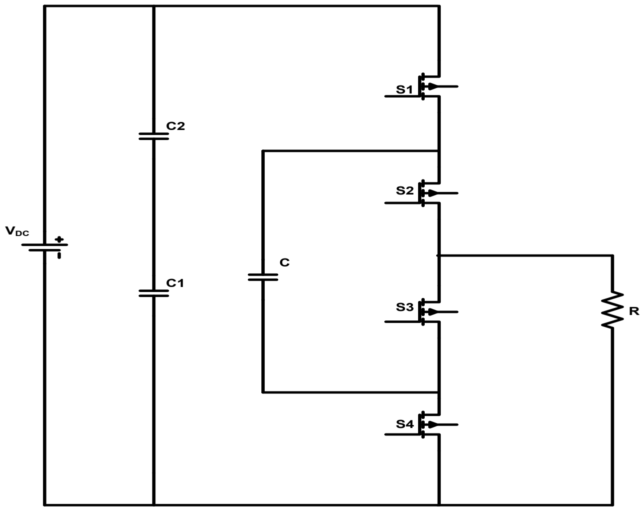

Fig -2: Flying Capacitor Multilevel Inverter

2.3 Cascaded H Bridge Multilevel Inverter

Fig. 2.3 shows the basic H-Bridge inverter circuit, which is the fundamental building block used in a Cascaded H-Bridge Multilevel Inverter (CHBMLI). The circuit consists of four power semiconductor switches (S1, S2, S3, and S4) arranged in an H-shaped configuration, along with a DC voltage source (Vdc) and a load connected between the midpoint of the two switch legs. The operation of the H-bridge inverter is based on controlling the switching states of these four switches to generate different voltage polarities across the load. When switches S1 and S4 are turned ON while S2 and S3 are OFF, the load receives a positive voltage (+Vdc). When switches S2 and S3 are turned ON while S1 and S4 are OFF, the polarity across the load reverses and the output becomes −Vdc. If switches S1 and S2 or S3 and S4 are turned ON simultaneously, the output voltage across the load becomes zero.

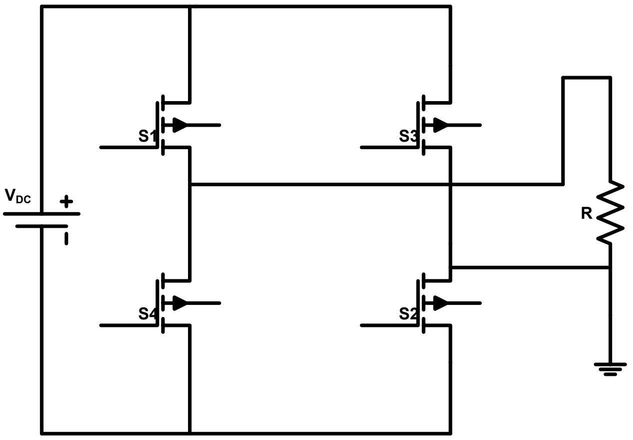

Fig -3: H Bridge Inverter circuit

In a Cascaded H-Bridge Multilevel Inverter, multiple H-bridge cells like the one shown in the figure are connected in series, each supplied by a separate DC source. By combining the output voltages of several H-bridge cells, the inverter can generate multiple stepped voltage levels such as +Vdc, +Vdc/2, 0, −Vdc/2, and −Vdc, depending on the number of cells used. This stepped waveform closely approximates a sinusoidal waveform, which significantly reduces harmonic distortion and improves power quality. The modular structure of the cascaded H-bridge inverter makes it easy to increase the number of voltage levels by simply adding more H-bridge cells, which is why this topology is widely used in motor drives.

3.1 Diode Clamped Multilevel Inverter

The figure 4 illustrates the MATLAB/Simulink model of a three-level diode-clamped multilevel inverter (DCMLI) along with its control circuitry and output measurement system. The left section of the model represents the control signal generation unit, where a sine wave acts as the reference signal for generating the desired AC output. Two repeating sequence blocks are used to generate carrier signals for pulse width modulation (PWM). These signals are compared using relational operator blocks, which determine the switching conditions by comparing the reference and carrier waveforms. The logical outputs from the comparators are processed using logical operator blocks to produce gate signals (s1, s2, s3, and s4). These signals are transmitted through Goto and from blocks to control the switching devices in the inverter circuit. The power Gui block is included to configure the simulation environment and enable the analysis of power electronic components within the MATLAB/Simulink platform.

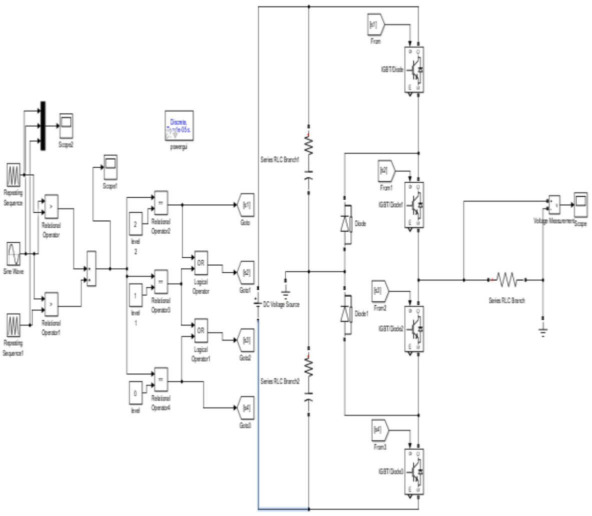

Fig -4: Diode Clamped Multilevel inverter in MATLAB Simulink

The right section of the model represents the power circuit of the diode-clamped multilevel inverter and the load system. A DC voltage source provides the input supply, which is divided using capacitive branches to create multiple voltage levels. The inverter consists of four IGBT switches with anti-parallel diodes, which are controlled by the gate signals generated in the control circuit. Additionally, clamping diodes are used to maintain voltage balance across the switches and to generate the intermediate voltage level required for three-level operation. By properly controlling the switching states of the IGBTs, the inverter produces three output voltage levels (+Vdc/2, 0, and −Vdc/2). The output is connected to a series RLC branch representing the load, and a voltage measurement block is used to monitor the output waveform through a scope. This simulation model demonstrates how a three-level diode-clamped multilevel inverter converts DC input into a stepped AC output with reduced harmonic distortion, thereby improving overall power quality.

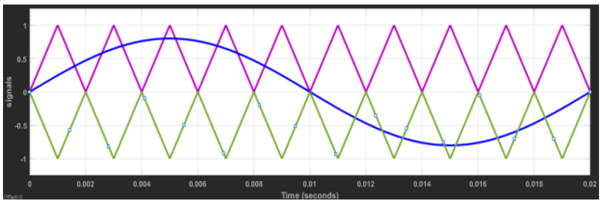

Fig -5: Reference and carrier signals used in the PWM switching scheme.

The figure 5 shows the comparison between the reference sine wave and the carrier triangular signals used for Pulse Width Modulation (PWM) in the multilevel inverter control system. The blue waveform represents the sinusoidal reference signal, which corresponds to the desired AC output waveform of the inverter. The magenta and green triangular waveforms represent the carrier signals that are used for generating switching pulses. This carrier signals operate at a higher frequency compared to the reference sine wave. By comparing the reference signal with the carrier signals using relational operators in the control circuit, switching pulses are generated to control the inverter switches. When the reference signal is greater than the carrier signal, the switching device turns ON, and when it is lower, the device turns OFF. This comparison process forms the basis of the PWM technique, which allows the inverter to produce a stepped output voltage that closely approximates a sinusoidal waveform. As a result, the harmonic distortion in the output voltage is reduced and the overall power quality of the multilevel inverter system is improved.

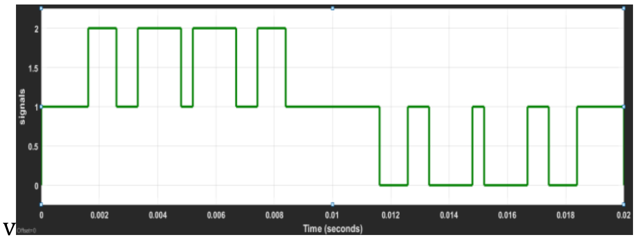

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Fig -6: Gate Pulse Signal Generated for the Inverter Switches

The figure 6 shows the switching signal waveform obtained from the output scope of the MATLAB/Simulink model used to control the multilevel inverter. The horizontal axis represents time in seconds, while the vertical axis represents the logic level of the switching signal generated by the control circuit. These signals are produced through the pulse width modulation (PWM) technique, where the reference sine wave is compared with carrier signals using relational and logical operators to generate gate pulses. The waveform indicates the ON and OFF states of the inverter switches, where higher logic levels represent the switching devices in the ON state and lower levels represent the OFF state. These switching pulses are applied to the IGBT switches in the inverter circuit, allowing the inverter to generate stepped voltage levels required for multilevel operation. The variation in pulse width over time helps in approximating a sinusoidal waveform at the output, thereby reducing harmonic distortion and improving the overall power quality of the inverter system.

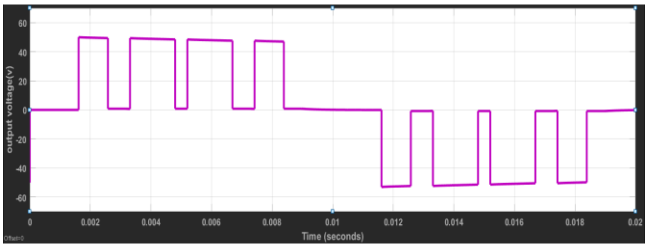


Fig -7: Output Voltage of Diode Clamped Multilevel Inverter

The figure 7 shows the output voltage waveform obtained from the MATLAB/Simulink simulation of the multilevel inverter. The horizontal axis represents time in seconds, while the vertical axis represents the output voltage in volts. The waveform exhibits a stepped voltage pattern, which is characteristic of multilevel inverter operation. During the positive half cycle, the output voltage switches between zero and a positive voltage level (approximately +50 V), while during the negative half cycle it switches between zero and a negative voltage level (approximately −50 V). These voltage levels are produced by controlling the switching states of the power semiconductor devices in the inverter using pulse width modulation (PWM) signals.

3.2 Flying Capacitor Multilevel Inverter

Fig. 8 illustrates the MATLAB/Simulink model of a three-level Flying Capacitor Multilevel Inverter (FCMLI) along with its PWM control circuit and load configuration. In the left section of the model, the control circuit generates switching signals using the Pulse Width Modulation (PWM) technique. A sine wave block acts as the reference signal representing the desired AC output waveform, while repeating sequence blocks generate high-frequency triangular carrier signals. These signals are compared using relational operator blocks, which produce PWM switching pulses. The generated gate signals are then transmitted through Goto and from blocks to control the switching devices in the inverter circuit.

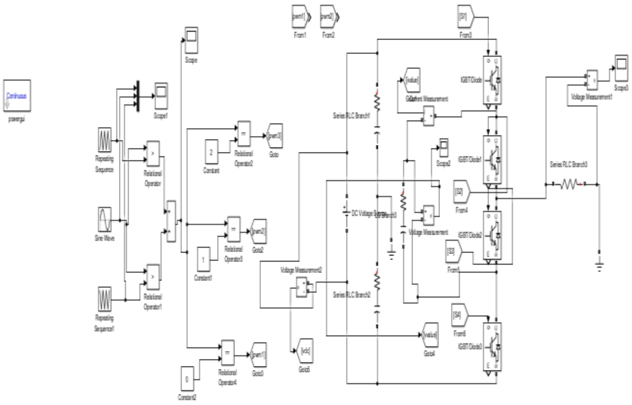


Fig -8: Flying Capacitor Multilevel inverter in MATLAB Simulink

The right section of the model represents the power circuit of the flying capacitor multilevel inverter. A DC voltage source provides the input supply, and the inverter consists of four IGBT switches with anti-parallel diodes (S1, S2, S3, and S4). A flying capacitor is connected between the switching nodes, which stores energy and helps generate intermediate voltage levels during switching operation. By properly controlling the switching states of the IGBTs using the PWM signals, the inverter produces three output voltage levels (+Vdc/2, 0, and −Vdc/2). The output is connected to a series

R load, and voltage measurement blocks and scope displays are used to observe the inverter output waveform. This configuration demonstrates how the flying capacitor multilevel inverter converts DC power into a stepped AC voltage with improved waveform quality and reduced harmonic distortion.

The figure 9 illustrates the reference and carrier signals used in the Pulse Width Modulation (PWM) control technique for the multilevel inverter. In the waveform, the red curve represents the sinusoidal reference signal, which corresponds to the desired AC output waveform of the inverter. The green and purple triangular waveforms represent the high-frequency carrier signals used for comparison in the PWM process. These carrier signals operate at a much higher frequency than the reference sine wave and are used to generate the switching pulses required for controlling the inverter switches.

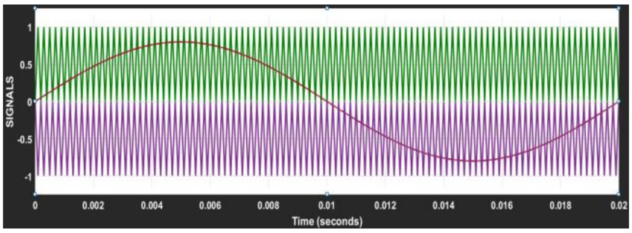


Fig -9: Carrier and reference signals used for PWM switching in the inverter control circuit.

During operation, the reference sine wave is continuously compared with the carrier triangular signals using comparator or relational operator blocks. When the reference signal is greater than the carrier signal, the corresponding switch is turned ON, and when it is lower, the switch is turned OFF. This comparison process generates the PWM gate signals required for the switching devices in the inverter circuit. The use of multiple carrier signals helps produce multiple voltage levels in the output waveform. As a result, the inverter can generate a stepped AC output that closely approximates a sinusoidal waveform, thereby reducing harmonic distortion and improving power quality in the multilevel inverter system.

The figure 10 shows the PWM gate pulse waveform generated for controlling the inverter switches in the multilevel inverter system. The horizontal axis represents time in seconds, while the vertical axis represents the logic level of the switching signal. The waveform consists of high-frequency pulses that alternate between different logic levels, indicating the ON and OFF states of the inverter switching devices. In the first half of the cycle, the switching pulses vary between higher logic levels, while in the second half they switch between lower levels, corresponding to the positive and negative halves of the reference sinusoidal signal used in the PWM control scheme.

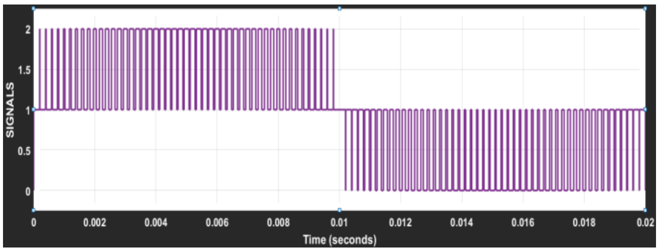


Fig -10: PWM control signal for the multilevel inverter switching operation.

These pulses are generated by comparing the reference sine wave with carrier triangular signals in the PWM control circuit. When the reference signal is greater than the carrier signal, the corresponding switch receives an ON pulse, and when it is lower, the switch turns OFF. The varying pulse widths indicate the pulse width modulation process, which controls the inverter switching pattern. These gate pulses are applied to the IGBT switches in the inverter circuit, enabling the generation of stepped output voltage levels. This switching technique helps the multilevel inverter produce an output waveform that approximates a sinusoidal waveform, thereby reducing harmonic distortion and improving the overall power quality.

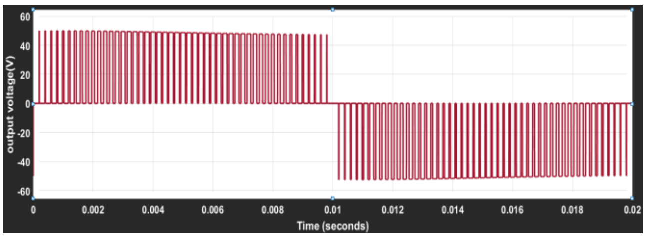


Fig -11: Output Voltage of Flying Capacitor Multilevel Inverter

The figure 11 shows the output voltage waveform obtained from the MATLAB/Simulink simulation of the multilevel inverter system. The horizontal axis represents time in seconds, while the vertical axis represents the output voltage in volts. The waveform consists of high-frequency pulses whose amplitude alternates between positive and negative voltage levels, indicating the inverter's switching operation. During the positive half cycle, the output voltage switches between 0 V and approximately +50 V, while during the negative half cycle it switches between 0 V and approximately −50 V. These pulses are produced by the PWM (Pulse Width Modulation) control technique, where switching devices such as IGBTs are turned ON and OFF according to the generated gate signals. The rapid switching creates a pulsed waveform that approximates a sinusoidal AC output when filtered or applied to the load. This switching pattern demonstrates how the inverter converts DC input voltage into an AC output voltage with controlled amplitude and reduced harmonic distortion, which is essential for improving power quality in multilevel inverter systems.

3.3 Cascaded H Bridge Multilevel Inverter

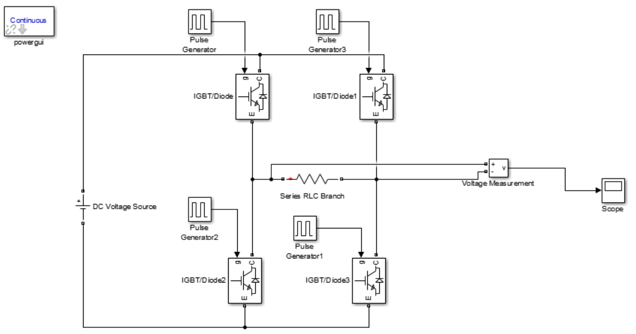


Fig -12: Cascaded H bridge Multilevel inverter in MATLAB Simulink

The figure 12 illustrates A cascaded H-bridge (CHB) 3-level inverter is a type of multilevel inverter that produces three distinct output voltage levels, namely +Vdc, 0, and −Vdc, using a single H-bridge cell in a single-phase configuration. The H-bridge consists of four power electronic switches, typically IGBTs with anti-parallel diodes, connected to a DC voltage source. By controlling the switching sequence, the inverter generates different voltage levels: when the diagonal switches (S1 and S4) are turned ON, the output is +Vdc; when the opposite diagonal switches (S2 and S3) are ON, the output becomes −Vdc; and when either the upper or lower pair of switches is activated, the output is zero. This stepped output waveform is closer to a sinusoidal waveform compared to a conventional two-level inverter, resulting in reduced harmonic distortion and improved power quality. The CHB topology is modular, efficient, and widely used in applications such as renewable energy systems, electric vehicles, and motor drives, although it requires proper switching control and, for higher levels, multiple isolated DC sources.

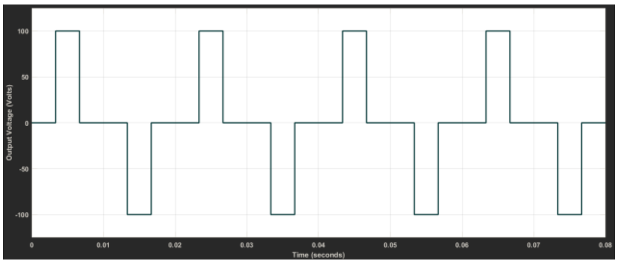


Fig -13: Output Voltage of Cascaded H Bridge Multilevel Inverter.

The figure 13 shows the output voltage waveform represents the output voltage of a three-level cascaded H-bridge (CHB) inverter, where the voltage alternates among +100 V, 0 V, and −100 V in a periodic sequence. This stepped waveform is produced by appropriate switching of the IGBTs in the H-bridge, such that the positive level is obtained when one diagonal pair of switches conducts, the negative level when the opposite pair conducts, and the zero level when either the upper or lower switches are turned on together. The presence of the zero state between positive and negative levels results in a waveform that is closer to a sinusoidal shape compared to a conventional two-level inverter, thereby reducing harmonic distortion and improving output quality. The waveform is symmetrical in both positive and negative halves, indicating balanced operation and a constant DC input, and its periodic nature corresponds to a typical fundamental frequency used in power applications.

4.2 THD of Diode Clamped multilevel inverter

The figure 14 illustrates both the time-domain output waveform of an inverter and its corresponding frequency-domain analysis using Fast Fourier Transform (FFT), providing a comprehensive understanding of the signal characteristics. In the upper portion of the figure, the inverter output voltage is shown as a stepped alternating waveform, which is typical of multilevel inverter configurations. The waveform alternates between positive and negative voltage levels with intermediate transitions, indicating controlled switching of power electronic devices such as IGBTs. A specific portion of the waveform, highlighted in red, is selected for FFT analysis, while the remaining part is shown in blue to represent the continuity of the signal over multiple cycles. This selection ensures accurate harmonic analysis by focusing on a steady-state segment of the waveform.

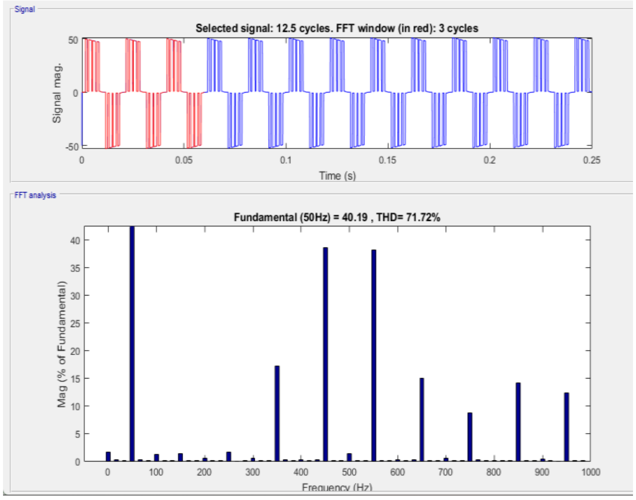
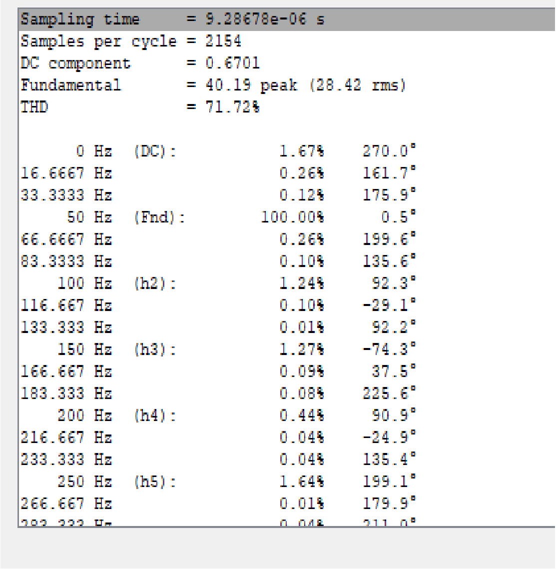


Fig -14: THD of Diode Clamped Multilevel Inverter In bar representation.

In the lower portion, the FFT spectrum presents the frequency components of the selected signal, where the horizontal axis represents frequency in hertz and the vertical axis indicates the magnitude of each harmonic component as a percentage of the fundamental. The fundamental frequency is observed at approximately 50 Hz, which is standard for many power systems, while multiple harmonic components appear at higher frequencies. The Total Harmonic Distortion (THD) is calculated to be around 71.2%, which is relatively high and indicates that the waveform deviates significantly from an ideal sinusoidal shape. Such a high THD implies the presence of strong harmonic components that can lead to increased power losses, and reduced overall efficiency of the system.

The figure 15 presents the numerical FFT analysis results of the diode-clamped multilevel inverter output voltage. The sampling time is 9.28678 × 10^{-6} seconds, with 2154 samples per cycle, ensuring accurate harmonic evaluation. The fundamental component at 50 Hz has a peak value of 40.19 V and an RMS value of 28.42 V. The table also lists the magnitude and phase angles of various harmonic components such as second, third, fourth, and fifth harmonics. These harmonics arise due to the switching characteristics of the diode-clamped inverter. FFT analysis is used to evaluate the harmonic performance and power quality of the DCMLI system, and the THD value provides an indication of the distortion present in the inverter output waveform.



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Sampling time     = 9.28678e-06 s
Samples per cycle = 2154
DC component      = 0.6701
Fundamental       = 40.19 peak (28.42 rms)
THD               = 71.72%

      0 Hz  (DC):         1.67%    270.0°
16.6667 Hz                0.26%    161.7°
33.3333 Hz                0.12%    175.9°
     50 Hz  (Fnd):      100.00%      0.5°
66.6667 Hz                0.26%    199.6°
83.3333 Hz                0.10%    135.6°
    100 Hz  (h2):         1.24%     92.3°
116.667 Hz                0.10%    -29.1°
133.333 Hz                0.01%     92.2°
    150 Hz  (h3):         1.27%    -74.3°
166.667 Hz                0.09%     37.5°
183.333 Hz                0.08%    225.6°
    200 Hz  (h4):         0.44%     90.9°
216.667 Hz                0.04%    -24.9°
233.333 Hz                0.04%    135.4°
    250 Hz  (h5):         1.64%    199.1°
266.667 Hz                0.01%    179.9°
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Fig -15: THD of Diode Clamped Multilevel Inverter In list representation.

4.2 THD of Flying Capacitor multilevel inverter

The figure 16 shows the FFT (Fast Fourier Transform) analysis of the output voltage waveform of the Flying Capacitor Multilevel Inverter (FCMLI) obtained from the MATLAB/Simulink simulation. The upper plot presents the time-domain waveform of the inverter output voltage, where a portion of the signal is selected for harmonic analysis. The red-highlighted section indicates the FFT analysis window, which contains three cycles of the waveform used to compute the harmonic spectrum. The lower graph illustrates the frequency spectrum of the output voltage, where the magnitude of each harmonic component is plotted against frequency. The analysis shows that the fundamental frequency of the inverter output is 50 Hz with a magnitude of 39.97, and the calculated Total Harmonic Distortion (THD) is 76.59%, indicating the presence of significant harmonic components in the waveform.

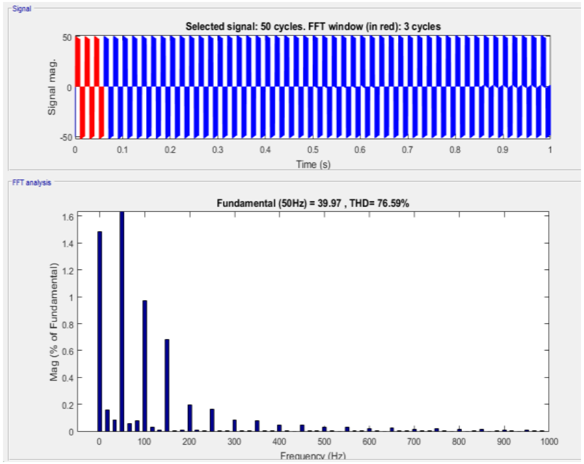
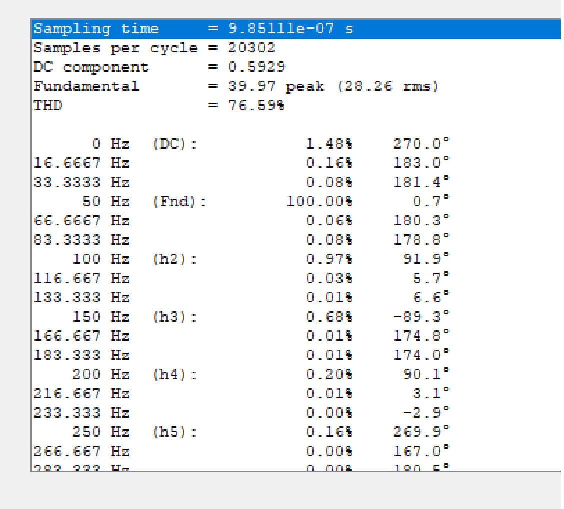


Fig -16: THD of Flying Capacitor Multilevel Inverter In bar representation.

The Fig 17 represents numerical FFT results provide additional details about the harmonic content of the flying capacitor multilevel inverter output voltage. The sampling time is 9.85111 × 10^{-7} seconds, with 20302 samples per cycle, ensuring high accuracy in frequency analysis. The fundamental component at 50 Hz has a peak value of 39.97 V and an RMS value of 28.26 V.



```
Sampling time     = 9.85111e-07 s
Samples per cycle = 20302
DC component      = 0.5929
Fundamental       = 39.97 peak (28.26 rms)
THD               = 76.59%

      0 Hz  (DC):         1.48%    270.0°
16.6667 Hz                0.16%    183.0°
33.3333 Hz                0.08%    181.4°
     50 Hz  (Fnd):      100.00%      0.7°
66.6667 Hz                0.06%    180.3°
83.3333 Hz                0.08%    178.8°
    100 Hz  (h2):         0.97%     91.9°
116.667 Hz                0.03%      5.7°
133.333 Hz                0.01%      6.6°
    150 Hz  (h3):         0.68%    -89.3°
166.667 Hz                0.01%    174.8°
183.333 Hz                0.01%    174.0°
    200 Hz  (h4):         0.20%     90.1°
216.667 Hz                0.01%      3.1°
233.333 Hz                0.00%     -2.9°
    250 Hz  (h5):         0.16%    269.9°
266.667 Hz                0.00%    167.0°
```

Fig -17: THD of Flying Capacitor Multilevel Inverter In list representation.

The table also lists the magnitude and phase angles of several harmonic components such as 100 Hz (second harmonic), 150 Hz (third harmonic), 200 Hz (fourth harmonic), and 250 Hz (fifth harmonic). These harmonics are generated due to the switching action of the inverter devices and the PWM control technique used in the flying capacitor topology. The FFT analysis is therefore used to evaluate the harmonic performance and power quality of the flying capacitor multilevel inverter, and the THD value of 76.59% indicates the level of distortion present in the inverter output waveform.

4.2 THD of Cascaded H Bridge Multilevel Inverter

The figure 18 illustrate the FFT (Fast Fourier Transform) analysis of the output voltage waveform of the Cascaded H-Bridge Multilevel Inverter (CHBMLI) obtained from the MATLAB/Simulink simulation. The upper plot shows the time-domain output voltage waveform, where a portion of the signal is selected for harmonic analysis. The red-highlighted section represents the FFT analysis window, which contains three cycles of the waveform used to determine the harmonic spectrum. The stepped waveform clearly indicates the multilevel nature of the cascaded H-bridge inverter, where multiple H-bridge cells combine to produce several voltage levels that approximate a sinusoidal waveform.

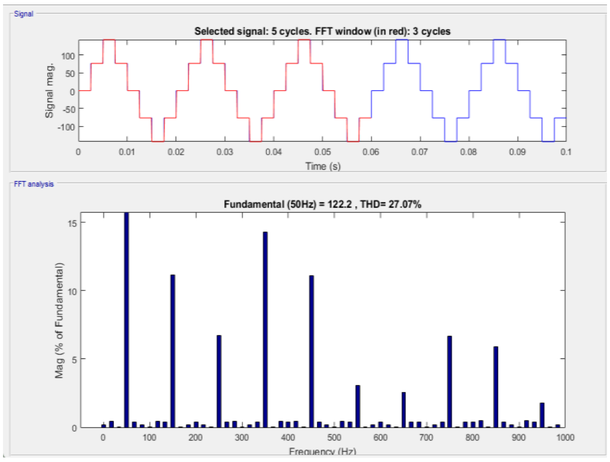
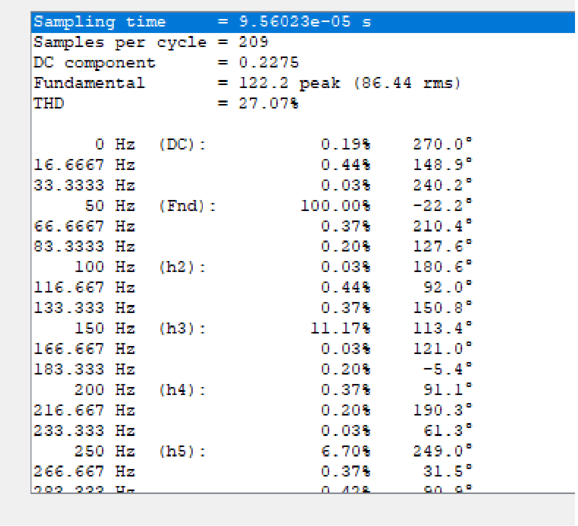


Fig -18: THD of Cascaded H Bridge Multilevel Inverter in Bar representation.

The lower graph presents the frequency spectrum of the output voltage, where the magnitude of each harmonic component is plotted with respect to frequency. The analysis shows that the fundamental frequency is 50 Hz with a magnitude of 122.2, and the calculated Total Harmonic Distortion (THD) is 27.07%, indicating a significant reduction in harmonic distortion compared to other inverter topologies.

The figure 19 illustrates numerical FFT results provide detailed information about the harmonic components present in the cascaded H-bridge multilevel inverter output voltage. The sampling time is 9.56023 × 10^{-5} seconds, with 209 samples per cycle used in the analysis. The fundamental component at 50 Hz has a peak value of 122.2 V and an RMS value of 86.44 V. The harmonic table lists the magnitude and phase angles of several harmonics such as 150 Hz (third harmonic), 200 Hz (fourth harmonic), and 250 Hz (fifth harmonic). These harmonics arise due to the switching operation of the MOSFET devices in each H-bridge cell. Compared with other multilevel inverter topologies, the cascaded H-bridge inverter produces a lower THD value of 27.07%, demonstrating improved waveform quality and better power quality performance due to its ability to generate multiple voltage levels at the output.



```
Sampling time      = 9.56023e-05 s
Samples per cycle = 209
DC component      = 0.2275
Fundamental       = 122.2 peak (86.44 rms)
THD               = 27.07%

      0 Hz   (DC):          0.19%    270.0°
16.6667 Hz                  0.44%    148.9°
33.3333 Hz                  0.03%    240.2°
     50 Hz   (Fnd):       100.00%    -22.2°
66.6667 Hz                  0.37%    210.4°
83.3333 Hz                  0.20%    127.6°
    100 Hz   (h2):          0.03%    180.6°
116.667 Hz                  0.44%     92.0°
133.333 Hz                  0.37%    150.8°
    150 Hz   (h3):         11.17%    113.4°
166.667 Hz                  0.03%    121.0°
183.333 Hz                  0.20%     -5.4°
    200 Hz   (h4):          0.37%     91.1°
216.667 Hz                  0.20%    190.3°
233.333 Hz                  0.03%     61.3°
    250 Hz   (h5):          6.70%    249.0°
266.667 Hz                  0.37%     31.5°
```

Fig -19: THD of Cascaded H Bridge Multilevel Inverter In list representation.

The figure shows a bar graph representing the Total Harmonic Distortion (THD) comparison of different multilevel inverter topologies obtained from MATLAB/Simulink simulation results. The horizontal axis represents the three inverter types: Diode-Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI), and Cascaded H-Bridge Multilevel Inverter (CHBMLI), while the vertical axis represents the THD percentage of the output voltage waveform. From the graph, the flying capacitor multilevel inverter exhibits the highest THD of 76.59%, followed by the diode-clamped multilevel inverter with 71.72% THD, indicating higher harmonic distortion in their output waveforms. In contrast, the cascaded H-bridge multilevel inverter shows the lowest THD value of 27.07%, which means it produces a waveform that is closer to a sinusoidal signal. This comparison demonstrates that the cascaded H-bridge inverter provides better harmonic performance and improved power quality compared to the diode-clamped and flying capacitor inverter topologies.

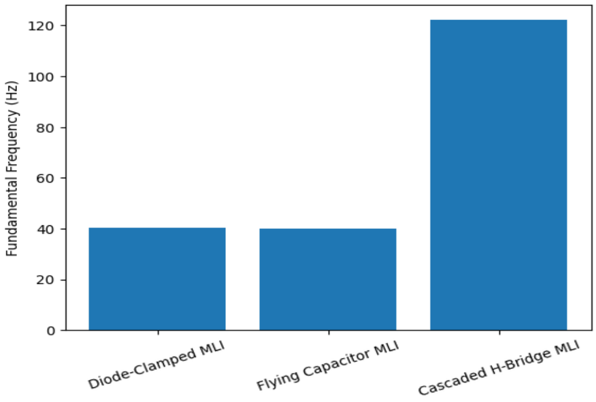


Fig -20: Fundamental Frequency Comparison of Multilevel Inverters.

The figure 20 shows a bar graph representing the fundamental frequency comparison of different multilevel inverter topologies obtained from simulation results. The horizontal axis indicates the three inverter types: Diode-Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI), and Cascaded H-Bridge Multilevel Inverter (CHBMLI), while the vertical axis represents the fundamental frequency in Hertz (Hz). From the graph, both the diode-clamped and flying capacitor multilevel inverters operate at approximately 40 Hz, showing similar fundamental frequency characteristics. In contrast, the cascaded H-bridge multilevel inverter produces a higher fundamental frequency of about 122.2 Hz.

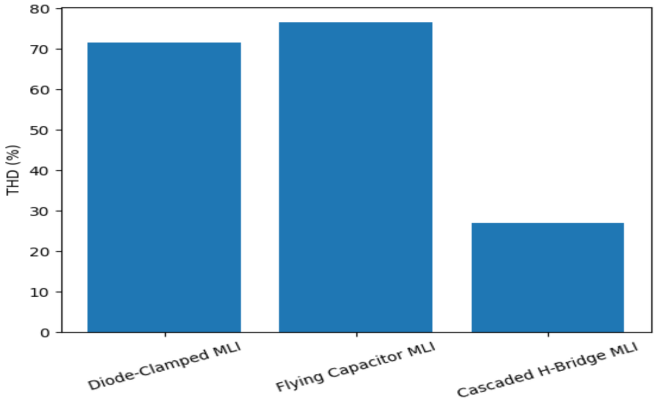


Fig -21: THD Comparison of Multilevel Inverter Topologies.

This comparison highlights the difference in output frequency characteristics among the three inverter topologies and indicates that the cascaded H-bridge inverter provides a higher fundamental frequency in the simulated system, which contributes to improved waveform formation when combined with its lower harmonic distortion.

3. CONCLUSIONS

In this project, the performance of three multilevel inverter topologies—Diode-Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI), and Cascaded H-Bridge Multilevel Inverter (CHBMLI)—was analyzed and compared using MATLAB/Simulink simulation, with Total Harmonic Distortion (THD) as the main comparison parameter. The simulation results and FFT analysis showed that multilevel inverters produce stepped output voltage waveforms that closely approximate a sinusoidal waveform, thereby improving power quality. Among the three topologies, the Cascaded H-Bridge Multilevel Inverter exhibited better harmonic performance with lower THD compared to the diode-clamped and flying capacitor inverters. Multilevel inverters provide several advantages such as reduced harmonic distortion, improved output voltage quality, lower switching stress on power devices, and reduced electromagnetic interference. They also allow high-voltage operation using lower-rated semiconductor devices, which improves system efficiency and reliability. Due to these advantages, multilevel inverters are widely used in applications such as renewable energy systems, motor drives, electric vehicles, and high-power industrial power conversion systems.

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