International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 13 Issue: 05 | May 2026 www.irjet.net p-ISSN: 2395-0072

A Comprehensive Review on Low-Power High-Speed XOR/XNOR Gate Design Techniques in VLSI Systems

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Abstract – *The rapid scaling of Very Large-Scale Integration (VLSI) technology has significantly increased the demand for energy-efficient and high-speed digital circuits. Among fundamental logic components, Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates play a critical role in arithmetic units, multipliers, and cryptographic systems. Their performance directly influences the overall efficiency of digital datapaths. Over the years, various design techniques such as static CMOS, pass-transistor logic, dynamic CMOS, hybrid logic, and multi-threshold CMOS (MTCMOS) have been proposed to optimize power consumption, delay, and area. However, each technique presents trade-offs in terms of leakage power, noise margin, and robustness. This paper presents a comprehensive review of existing XOR/XNOR gate design methodologies, analyzing their advantages, limitations, and performance characteristics. Furthermore, emerging approaches such as conditional keeper techniques, compute-in-memory architectures, and nanoscale devices are also discussed. Finally, key research gaps and future directions are identified to guide the development of next-generation ultra-low-power arithmetic circuits.*

Key Words: XOR/XNOR, VLSI, Dynamic CMOS, MTCMOS, Low Power Design, Hybrid Logic, PDP, Leakage Reduction

1. INTRODUCTION

With continuous scaling in semiconductor technology, modern digital systems demand high-speed operation along with minimal power consumption. The breakdown of traditional scaling laws has led to increased leakage currents and thermal issues, making energy efficiency a critical design parameter.

XOR and XNOR gates are fundamental building blocks in arithmetic circuits such as adders, multipliers, and cryptographic modules. These gates often lie on the critical path of computation, making their optimization essential for improving overall system performance.

This review paper presents a detailed analysis of various XOR/XNOR design techniques, highlighting their strengths, limitations, and suitability for modern VLSI systems.

2. CLASSIFICATION OF XOR/XNOR DESIGN TECHNIQUES

XOR/XNOR gates can be broadly classified based on logic styles:

2.1 Static CMOS Logic

Static CMOS logic is the most widely adopted design style due to its robustness and ability to provide full voltage swing at the output. It consists of complementary pull-up (PMOS) and pull-down (NMOS) networks, ensuring reliable operation under varying conditions.

The primary advantage of static CMOS logic lies in its high noise immunity and stable operation, making it suitable for critical applications. However, XOR/XNOR implementations using static CMOS typically require around 16 transistors, leading to increased input capacitance and higher dynamic power consumption. As a result, this logic style is less efficient for high-speed and low-power applications.

2.2 Pass Transistor Logic (PTL)

Pass Transistor Logic (PTL) reduces the number of transistors by eliminating redundant PMOS devices and using transistors as switches to pass logic levels. This results in compact designs with reduced area and lower power consumption.

Despite these advantages, PTL suffers from threshold voltage loss, which leads to degraded output voltage levels. This degradation affects noise margin and limits its applicability in cascaded logic circuits. Additionally, PTL designs face scalability issues in deep sub-micron technologies due to increased leakage currents.

2.3 Dynamic CMOS Logic

Dynamic CMOS logic operates using two phases: precharge and evaluation, controlled by a clock signal. During the precharge phase, the output node is charged to a known state, while in the evaluation phase, the logic function is evaluated.

This logic style offers high-speed operation due to reduced input capacitance and fewer transistors. However, dynamic CMOS suffers from several inherent issues such as charge sharing, leakage current, and keeper contention. These problems can lead to incorrect logic evaluation and increased power dissipation, especially in nanoscale technologies.

2.4 Hybrid Logic Styles

Hybrid logic combines different logic styles such as static CMOS, pass transistor logic, and transmission gates to achieve optimized performance. These designs aim to balance power consumption, delay, and area by leveraging the strengths of multiple techniques.

Hybrid XOR/XNOR circuits typically achieve improved Power-Delay Product (PDP) compared to conventional designs. However, the increased complexity in circuit design and layout makes implementation challenging, especially for large-scale integration.

2.5 Multi-Threshold CMOS (MTCMOS) Technique

MTCMOS is a widely used leakage reduction technique in modern VLSI systems. It employs both low-threshold (low-Vth) and high-threshold (high-Vth) transistors within the same circuit. Low-Vth transistors are used in critical paths to maintain high speed, while high-Vth transistors are used as sleep transistors to reduce leakage power during standby mode.

This technique significantly reduces subthreshold leakage current, making it highly suitable for low-power applications. However, it introduces additional area overhead and requires control circuitry for managing sleep modes.

3. REVIEW OF EXISTING WORKS

Several researchers have contributed to improving XOR/XNOR gate performance.

Goel *et al.* proposed hybrid CMOS full adder designs that improved energy efficiency but increased complexity.

Kao and Chandrakasan introduced MTCMOS techniques that significantly reduced leakage power in nanoscale circuits.

Mishra *et al.* developed high-speed XOR/XNOR circuits but faced voltage degradation issues.

Naseri and Timarchi proposed optimized XOR/XNOR-based full adders achieving improved PDP.

Nikoubin *et al.* introduced three-input XOR/XNOR gates with reduced transistor count and improved area efficiency.

Yadav *et al.* focused on PVT-resilient XOR/XNOR designs, improving robustness under process variations.

Recent works emphasize hybrid logic, reduced transistor count, and leakage reduction techniques, but trade-offs still exist between speed, power, and reliability.

4. COMPARATIVE ANALYSIS

Table 1: Comparison of XOR/XNOR Design Techniques

Technique	Speed	Power	Area	Limitation
Static CMOS	Low	High	High	Large capacitance
PTL	Medium	Low	Low	Voltage degradation
Dynamic CMOS	High	Medium	Low	Leakage & contention
Hybrid Logic	High	Medium	Medium	Complexity

5. EMERGING TRENDS IN XOR/XNOR DESIGN

With the continuous scaling of CMOS technology into deep sub-micron and nanometer regimes, conventional logic design techniques face significant challenges such as increased leakage power, reduced noise margins, and reliability degradation. To address these issues, several emerging design approaches have been proposed to enhance the performance of XOR/XNOR circuits.

5.1 Conditional Keeper Techniques

Conditional keeper techniques have been introduced to overcome one of the major limitations of dynamic CMOS logic, namely keeper contention. In conventional dynamic circuits, the keeper transistor maintains logic levels but introduces short-circuit current when the pull-down network is active.

The conditional keeper approach dynamically controls the keeper transistor, disabling it during the evaluation phase and enabling it afterward. This significantly reduces contention current and improves switching speed. Studies have shown that this technique can reduce Power-Delay Product (PDP) by up to 40–60% compared to conventional dynamic logic.

5.2 Compute-in-Memory (CIM) Architectures

Compute-in-Memory (CIM) is an emerging paradigm that integrates computation within memory arrays, thereby reducing the need for data transfer between memory and processing units. Since data movement contributes significantly to overall energy consumption, CIM architectures offer substantial improvements in energy efficiency.

In XOR/XNOR applications, CIM enables direct implementation of logic operations within SRAM or non-volatile memory cells. This approach can reduce energy consumption by approximately 40–70% compared to conventional von Neumann architectures, making it highly suitable for AI accelerators and edge computing systems.

5.3 FinFET and CNTFET Technologies

As planar CMOS approaches its scaling limits, advanced device technologies such as FinFET and Carbon Nanotube Field-Effect Transistors (CNTFETs) have emerged as promising alternatives.

FinFET devices provide better electrostatic control over the channel, significantly reducing short-channel effects and leakage current. Similarly, CNTFETs offer near-ballistic transport and superior carrier mobility, enabling high-speed operation with reduced power consumption.

These technologies enable XOR/XNOR designs with improved energy efficiency, reduced leakage, and better scalability for future technology nodes below 10 nm.

5.4 Gate Diffusion Input (GDI) Technique

The Gate Diffusion Input (GDI) technique is an efficient method for designing low-power digital circuits with reduced transistor count. Unlike conventional CMOS logic, GDI allows multiple inputs to be applied at the source and gate terminals of transistors, enabling the realization of complex logic functions with fewer components.

GDI-based XOR/XNOR circuits can achieve transistor counts as low as 6–8 transistors while maintaining acceptable performance. This leads to reduced switching activity, lower dynamic power consumption, and improved overall efficiency. However, GDI designs may suffer from threshold voltage loss and require careful biasing for reliable operation.

6. RESEARCH GAP

Despite significant advancements in XOR/XNOR gate design techniques, several critical challenges remain unresolved, particularly in the context of deep sub-micron and nanoscale VLSI technologies.

One of the primary challenges is the **simultaneous optimization of power consumption, propagation delay, and circuit robustness**. Most existing designs focus on improving one or two performance parameters, often at the expense of others. For instance, pass transistor logic and hybrid designs reduce transistor count and power consumption but suffer from degraded voltage levels and reduced noise margins. Conversely, static CMOS ensures robustness and full voltage swing but results in higher power consumption and increased delay due to larger capacitance.

Another major concern is **leakage power dissipation**, which has become dominant in nanoscale technologies due to reduced threshold voltages and increased subthreshold conduction. Although techniques such as MTCMOS have been proposed to mitigate leakage, they introduce additional design complexity, area overhead, and control circuitry requirements, limiting their widespread adoption in compact designs.

Dynamic CMOS logic, while offering high-speed operation, suffers from inherent limitations such as **keeper contention and charge sharing**. The presence of a keeper transistor, although necessary for maintaining logic levels, leads to short-circuit current during the evaluation phase, thereby increasing power consumption and delay. Existing designs have not fully addressed this contention problem without compromising circuit stability.

Furthermore, **reduced-transistor XOR/XNOR implementations**, which aim to minimize area and power, often fail to maintain full voltage swing at the output. This results in degraded signal integrity, poor noise margins, and reduced reliability when cascaded in larger digital systems.

In addition, many existing works do not adequately consider **process, voltage, and temperature (PVT) variations**, which significantly affect circuit performance and reliability in modern technology nodes. The lack of robust designs capable of maintaining consistent performance under varying conditions remains a key limitation.

Motivation for Proposed Work

To address the aforementioned challenges, there is a need for a design approach that integrates:

- High-speed operation of dynamic CMOS logic
- Leakage reduction capability of MTCMOS
- Contention-free operation using conditional keeper techniques
- Full voltage swing and improved noise margins

Therefore, the proposed work focuses on developing an **energy-efficient dynamic CMOS XOR/XNOR gate** that combines conditional keeper and multi-threshold techniques to achieve improved power-delay performance while ensuring robustness and reliability.

7. FUTURE DIRECTIONS

The continuous evolution of VLSI technology and the increasing demand for energy-efficient digital systems open several promising directions for future research in XOR/XNOR gate design.

One important direction is the **integration of dynamic CMOS logic with MTCMOS techniques** to achieve simultaneous optimization of speed and leakage power. While dynamic logic provides high-speed operation due to reduced capacitance, MTCMOS enables effective suppression of subthreshold leakage currents. The combined implementation of these techniques, along with advanced control strategies such as conditional keeper mechanisms, can significantly enhance overall circuit performance.

Another promising area is the adoption of **emerging device technologies such as FinFET and CNTFET**. FinFET structures offer improved electrostatic control over the channel, thereby reducing short-channel effects and leakage currents. Similarly, CNTFET-based designs provide near-ballistic transport and high carrier mobility, enabling ultra-low-power and high-speed operation. These technologies are expected to play a crucial role in future nanoscale XOR/XNOR circuit implementations.

8. CONCLUSIONS

This paper presented a comprehensive review of XOR/XNOR gate design techniques in VLSI systems. Various logic styles including static CMOS, dynamic CMOS, hybrid logic, and MTCMOS were analyzed. Each technique offers unique advantages and limitations, making trade-offs unavoidable. Emerging techniques such as conditional keeper and compute-in-memory show promising potential for future low-power designs. The review highlights key research gaps and provides directions for developing next-generation energy-efficient digital circuits.

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