

# Power Quality Improvement In Distribution System By Using An Inverter Based UPQC With Reduced DC Link Voltage Rating

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**Abstract -** This paper proposes a new concept for mitigating harmonics and power quality issues by using UPQC. Without comprising its compensation capacity, the proposed UPQC topology reduces the dc-link voltage. The proposed topology uses a dc-link capacitor in series with interfacing inductor and also the neutral terminal of the system is connected to the negative terminal of the dc-link voltage for eliminating the fourth leg of the VSI of the shunt active filter. In the VSI based UPQC, decreases the average switching frequency of the switches and also switching losses in the inverter. UPQC is a custom device for improving the quality and reliability of the electrical system. In this paper discuss the series capacitor design and VSI parameters of UPQC topology. Three-phase five level diode clamped inverter based UPQC is designed for improving power quality performance and also reduces the total harmonic distortion. Simulation results was carried out by simulink/MATLAB software.

**Key Words:** Unified power quality conditioner (UPQC), voltage source inverter (VSI), total harmonic distortion (THD), power quality, DC-link voltage, three-phase five-level diode clamped inverter.

## 1. INTRODUCTION

In recent years, the power distribution system becoming highly exposed to the different power quality issues. The utilization of the power electronic devices are rising concern and is being connected to the distribution system. Unified Power Quality Conditioner is an effective device which consist of two inverters connected in back-to-back with both supply voltage and load current and acts as a series and shunt active power filters. Dynamic Voltage Restorer (DVR) is called as series part of the UPQC and Distribution Static Compensator (DSTATCOM) is called as shunt part of the UPQC. DVR compensates the voltage unbalance, voltage swells, voltage harmonics and voltage flickers. DSTATCOM compensates reactive currents current harmonics and free distortion with unity power factor.

The dc-link voltage has higher value of the line-to-neutral voltage for shunt active filter [2]. The topology uses the capacitor in series with the interfacing inductor of the shunt active filter and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter of the shunt active filter [5].

The series and shunt active filters dc-link voltage requirements match with a dc-link common capacitor [13]. The shunt active filter of voltage source inverter (VSI) fourth leg avoids and shunt VSI of each leg with single dc capacitor enables with independent control.

In three-phase four-wire system, neutral clamped topology is used for UPQC. The voltage balancing of the capacitor avoids this topology [19]. To eliminate the four-leg topology problems, a three-phase VSC based DSTATCOM and T-connected transformer are proposed. Because of extra transformer, this topology increases the bulkiness and the cost of the UPQC.

## 2. CONVENTIONAL TOPOLOGY OF UPQC

Considering a neutral clamped VSI based UPQC for conventional topology as shown in fig.1. This topology consist of two storage dc devices, the VSI of each leg is independently controlled. When compared to other VSI topologies, the tracking is smooth with less number of switches.

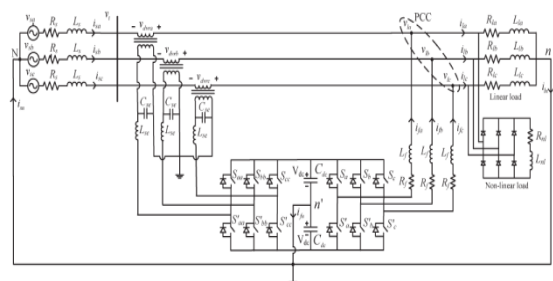


Fig.1. Equivalent circuit of neutral-clamped VSI topology-based UPQC

The source voltages of phases a, b and c can be represented by  $v_{sa}, v_{sb}$  and  $v_{sc}$ . The terminal voltages are taken as  $v_{ta}, v_{tb}$  and  $v_{tc}$ . Voltages of the series active power filters are  $v_{dvra}, v_{dvrb}$  and  $v_{dvrc}$ .  $i_{sa}, i_{sb}$  and  $i_{sc}$  are three-phase source currents,  $i_{la}, i_{lb}$  and  $i_{lc}$  are load currents,  $i_{fa}, i_{fb}$  and  $i_{fc}$  are the currents of shunt active filters and the current in the neutral line is  $i_{ln}$ . The feeder resistance and inductance are represented by  $R_s$  and  $L_s$ .  $R_f$  and  $L_f$  are the interfacing resistance and inductance of the shunt active filter. Similarly  $C_{se}$  and  $L_{se}$  are the filter capacitor and interfacing inductor of the series active filter.

### 3. PROPOSED TOPOLOGY OF UPQC

The equivalent circuit of the proposed VSI topology for UPQC compensated system is shown in fig.2. In this proposed topology, the system neutral is connected to the dc bus of the positive terminal with the capacitor  $C_f$  in series and also an interfacing inductance of the shunt active filter. The proposed topology is called as modified topology.

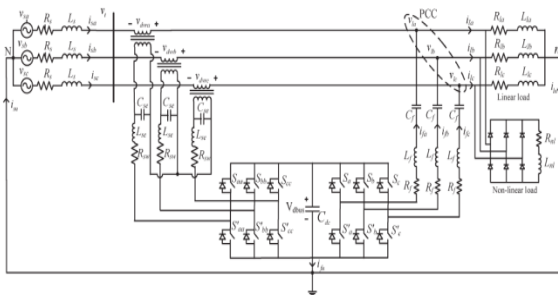


Fig.2. Equivalent circuit of proposed VSI topology for UPQC compensated system

This paper shows the load consists of both non-linear and linear loads.  $C_{dc1}=C_{dc2}=C_{dc}$  are the dc-link capacitor voltages and  $V_{dc1}=V_{dc2}=V_{dc}$  are the voltages across the dc-link capacitors. Finally  $V_{dbus}$  ( $V_{dc1}+V_{dc2}=2V_{dc}$ ) is the total dc-link voltage. The  $C_f$  (passive capacitor) has the ability to inject the reactive power is balanced by the active filter, but the load generates the harmonics. The dc-link voltage decreases by using series capacitor with interfacing inductor of the shunt active filter. Therefore, average switching frequency of switches will be reduced.

### 4. DESIGN OF VSI PARAMETERS

For better tracking performance, the VSI (voltage source inverter) parameters are carefully designed. For series and shunt active filter, the VSI parameter design details are following equations.

#### 4.1 Design of Series Active Filter VSI Parameters

For designing the series active filter system, a resistor is connected in series with the filter capacitor for first order system referred as switching band-resistor ( $R_{sw}$ ).  $I_{inv}, I_l$  and  $I_{se}$  can be represented as series inverter current rating, load current and capacitor current. Therefore, the capacitor current rms value is  $I_{se} = \sqrt{I_{inv}^2 + I_l^2}$ . The fundamental current and  $I_{sw}$  is the frequency current. The capacitor current and DVR voltage are given below,

$$V_{ref1} = I_{se1} X_{se1} = \frac{I_{se1}}{2\pi f_1 C_{se}} \quad (3)$$

$$V_{sw} = I_{sw} R_{sw} = \frac{h_2}{\sqrt{3}} \quad (4)$$

where hysteresis band voltage is taken as  $h_2$ ,  $V_{ref1}$  is the fundamental reference voltage of  $I_{se1}$  and  $V_{sw}$  is the band voltage of  $I_{sw}$ .

The capacitance ( $C_{se}$ ) and the resistance ( $R_{sw}$ ) are expressed in terms of rated reference voltage ( $V_{ref1}$ ) and band voltage ( $V_{sw}$ ), are given below,

$$C_{se} = \frac{I_{se1}}{2\pi V_{ref1} f_1} \quad (5)$$

$$R_{sw} = \frac{h_2}{I_{sw} \sqrt{3}} \quad (6)$$

Based on the switching frequency, the interfacing inductor ( $L_{se}$ ) of the series active filter can be expressed as,

$$L_{se} = \frac{V_{bus} R_{sw}}{4 f_{swmax} h_2} \quad (7)$$

where total dc-link voltage across both the dc-link capacitor can be represented as  $V_{bus}$ . For conventional VSI topology, the system parameters are listed in Table 1

Table 1: System Parameters

System Quantities	Values
System voltages	230 V(line to neutral),50 Hz
Feeder impedance	$Z_s=1+j3.141 \Omega$
Linear Load	$Z_{la}=34+j47.5 \Omega$ , $Z_{lb}=81+j39.6 \Omega$ , $Z_{lc}=31.5+j70.9\Omega$ .
Nonlinear load	Three phase full bridge rectifier load feeding a R-L load of 150 $\Omega$ -300mH.
Shunt VSI parameter	$C_{dc}=2200\mu F$ , $L_f=26$ mH, $R_f=1 \Omega$ , $V_{dbus}=2 \times V_{dc}=1040$ V (Conventional), $V_{dbus}=560V$ (Proposed)
Series VSI parameter	$C_{se}=80\mu F$ , $L_{se}=5mH$ , $R_{sw}=1.5\Omega$
Series interfacing transformer	1:1,100 V and 700 VA
PI gains	$K_p=6$ , $K_i=5.5$
Hysteresis band	$h_1=\pm 0.5$ A, $h_2=\pm 6.9V$

### 4.2 Design of Shunt Active Filter VSI Parameters

For n cycles, the active filter is connected to an X kVA system and deals with 0.5X kVA and 2X kVA handling capacity is considered under transient conditions. In the transient conditions by increasing the system kVA load ,then the voltage across each dc-link capacitor( $V_{dc}$ ) is reduces.During transient,allowing a maximum of 25% variation in  $V_{dc}$ .The differential energy( $\Delta E_c$ ) across  $C_{dc}$  is given by

$$\Delta E_c = \frac{C_{dc} [(1.125 V_{dc})^2 - (0.875 V_{dc})^2]}{2} \quad (8)$$

When the load changes, system energy also changes from 2X kVA to 0.5X kVA is

$$\Delta E_s = (2X - X/2)nT \quad (9)$$

By equating the equations, the dc-link capacitor value is given by

$$C_{dc} = \frac{2(2X - X/2)nT}{(1.125V_{dc})^2 - (0.875V_{dc})^2} \quad (10)$$

Where X=kVA rating of the system

T=time period of each cycle

$V_m$ =peak value of the source voltage

n=number of cycles

For analyzing the VSI,the relationship between m and minimum( $f_{swmin}$ ),maximum switching frequency( $f_{swmax}$ ) is given below,

$$m = \frac{1}{\sqrt{1 - f_{swmin} / f_{swmax}}} \quad (11)$$

Consider the shunt interfacing inductance of the maximum frequency and is given by,

$$L_f = \frac{mV_m}{4h_1 f_{swmax}} \quad (12)$$

Where, k1 and k2 are represented as proportionality constants and h1 is the hysteresis band and is given below,

$$h_1 = \sqrt{\frac{k_1 (2m^2 - 1)}{k_2 4m^2} f_{swmax}} \quad (13)$$

### 4.3 Design of $C_f$ for the Proposed VSI Topology

In general, most of the electrical loads are combination of the non-linear and linear inductive loads .Currents of loads with nonlinear components are very rare. The proposed VSI topology can be work efficiently under these conditions. The design of  $C_f$  depends upon the dc-link voltage and is carried out by the maximum load current. If the maximum KVA rating, base voltage of the system is taken as  $S_{max}$  and  $V_{base}$  then the minimum impedance of the system is given below,

$$Z_{min} = \frac{V_{base}^2}{S_{max}} = |R_l + jX_l| \quad (14)$$

For executing an unity power factor system, current of the shunt active filter demands to supply the required load current of the reactive component. The load current and the filter current are given below,

$$I_{load} = \frac{V_{lt}}{R_l + jX_l} \quad (15)$$

$$I_{filter} = \frac{V_{inv1} - V_{lt}}{R_f + j(X_{lf} - X_{cf})} \quad (16)$$

where  $X_{cf} = \frac{1}{2\pi f C_f}$

$$X_{lf} = 2\pi f L_f$$

$$X_l = 2\pi f L_l$$

By eliminating an interfacing resistance and only equating the imaginary part of above equations,

$$\frac{V_{l1} X_l}{R_l^2 + X_l^2} = \frac{V_{inv1} - V_{l1}}{(X_{lf} - X_{cf})^2} (X_{lf} - X_{cf}) \quad (17)$$

where  $V_{l1}$  and  $V_{inv1}$  are the PCC voltage at the fundamental frequency and the line to neutral rms voltage of the inverter. The fundamental component of the inverter voltage ( $V_{inv1}$ ) in terms of dc-link voltage is given below,

$$V_{inv1} = \frac{0.612 V_{dc}}{2\sqrt{3}} \quad (18)$$

The filter current ( $i_f$ ) flows through the inverter terminal to the PCC the inverter terminal voltage must be at high

potential. In conventional topology, the dc-link voltage must be higher than the voltage at the PCC. KVL along the filter branch for proposed and conventional topology

$$uV_{dc} - v_l = L_f \frac{di_f}{dt} + R_f i_f \quad (19)$$

$$(uV_{dc} - \frac{1}{C_f} \int i_f dt) - v_l = L_f \frac{di_f}{dt} + R_f i_f \quad (20)$$

$$(uV_{dc} - v_{cf}) - v_l = L_f \frac{di_f}{dt} + R_f i_f \quad (21)$$

When the load is in inductive nature, the fundamental voltage across the capacitor ( $v_{cf1}$ ) combines with the inverter terminal voltage ( $uV_{dc}$ ) and also for reactive power compensation, the filter current leads the voltage at PCC by  $90^\circ$  and further the voltage across the capacitor lags  $I_f$  by  $90^\circ$ . Therefore  $v_{cf1}$  will be phase opposition with the  $v_{l1}$ . So, that the  $v_{cf1}$  combines with the  $uV_{dc}$ . Finally the dc-link voltage of proposed topology is low compared with the conventional topology. The system neutral is connected to the negative terminal of the dc bus capacitor in the modified topology and it will offers a positive component in the inverter output voltage. So that the  $+V_{dbus}$  occurs at the inverter output when the top switch is closed. But zero voltage occurs when bottom switch is closed. Then the inverter has dc output voltage component along with the ac voltage and also these results in the automatic tracking of the neutral current [6]. The series capacitor blocks the dc voltage and voltage across series capacitor consist of two components: ac component and dc component. But inverter output voltage varies between  $+V_{dc}$  and  $-V_{dc}$  when top switch and bottom switch is closed in case of conventional topology and also similar in case of four leg topology is used for shunt active filter. Therefore the modified topology has benefits of both the four leg inverter and neutral clamped topology.

## 5. GENERATION OF REFERENCE COMPENSATOR CURRENTS UNDER UNBALANCED AND DISTORTED VOLTAGES

The load currents are unbalanced and distorted, these currents flows to the feeder impedance and then makes the voltage at terminals unbalanced and distorted in this work. The voltage at PCC are balanced and sinusoidal by the series active filter. These voltage contains some distortions and switching frequency component. The shunt filter current are produced by these terminal voltage. The fundamental positive sequence of the PCC

voltages ( $v_{la1}^+(t)$ ,  $v_{lb1}^+(t)$  and  $v_{lc1}^+(t)$ ) are used for controlling the shunt active filter.

$$i_{fa}^* = i_{la} - i_{sa}^* = i_{la} - \frac{v_{la1}^+ + \gamma(v_{lb1}^+ - v_{lc1}^+)}{\Delta_1^+} (P_{avg} + P_{loss}) \quad (19)$$

$$i_{fb}^* = i_{lb} - i_{sb}^* = i_{lb} - \frac{v_{lb1}^+ + \gamma(v_{lc1}^+ - v_{la1}^+)}{\Delta_1^+} (P_{avg} + P_{loss}) \quad (20)$$

$$i_{fc}^* = i_{lc} - i_{sc}^* = i_{lc} - \frac{v_{lc1}^+ + \gamma(v_{la1}^+ - v_{lb1}^+)}{\Delta_1^+} (P_{avg} + P_{loss}) \quad (21)$$

$$\text{where } \Delta = \sum_{j=a,b,c} (v_{ij1}^+)^2$$

$$\gamma = \tan \frac{\varphi}{\sqrt{3}}$$

$\varphi$  = phase angle between the source voltage and current

The above equations  $P_{avg}$ ,  $P_{loss}$  represents the average load power, switching and ohmic losses are generated by using a capacitor voltage PI controller. The reference voltage for series active filter are as follows,

$$v_{dvr i}^* = v_{li}^* - v_{ti} \quad (22)$$

$$i = a, b, c$$

where  $v_{dvr i}^*$  = reference series active filter voltages

$v_{li}^*$  = load voltages in three phases

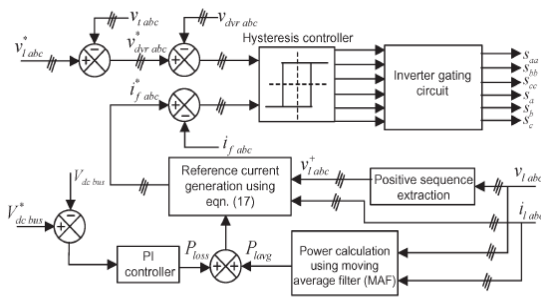


Fig.3.Control block diagram for UPQC

The control circuit of both the topologies is same and is shown in fig.3. Only six switching commands are to be generated. These six signals along with the complementary signals will control all the twelve switches of the two inverters.

The actual quantities and reference quantities are generated from the measurements. Using hysteresis band current method, the VSI switches of switching commands are obtained. Hysteresis current controller technique is feedback based loop, consist of two-level comparators. Whenever the error limit exceeds a specified tolerance band “±h”, the switching commands are appeared. The disadvantage of hysteresis controller is that the switching frequency of converter is highly dependent on the ac voltage and varies with it. The advantage of hysteresis controller has peak current limiting capacity and independence from load parameter variations.

The switching commands for shunt active filter is given as follows.

If  $i_{fa} \geq i_{fa}^* + h_1$ , then top switch is turned OFF and bottom switch is turned ON ( $S_a = 0, S'_a = 1$ ).

If  $i_{fa} \leq i_{fa}^* - h_1$ , then bottom switch is turned OFF and top switch is turned ON ( $S_a = 1, S'_a = 0$ ).

Similarly the switching control law for series active filter is given as follows.

If  $v_{dvra} \geq v_{dvra}^* + h_2$ , then top switch is turned OFF and bottom switch is turned ON ( $S_{aa} = 0, S'_{aa} = 1$ ).

If  $v_{dvra} \leq v_{dvra}^* - h_2$ , then bottom switch is turned OFF and top switch is turned ON ( $S_{aa} = 1, S'_{aa} = 0$ ).

### 6. THREE-PHASE FIVE-LEVEL CLAMPED INVERTER

In recent decade, three-phase five-level diode clamped inverter is very attractive due to their high efficiency, high voltage rating and high power rating is obtained without transformer.

The elementary concept of three-phase five-level diode clamped inverter, higher power is obtained by using a series connected power semi-conductor switches with lower voltage dc sources for performing power conversion by combining a stepped voltage waveform.

Batteries, capacitors and renewable voltage sources are used for multiple dc voltage sources. These multiple dc sources, the commutation of the power switches aggregated in order to obtain the higher output voltage. However, the voltage rating of the semi-conductor switches is depends upon the dc voltage source rating to which they are connected. It is not only generate the output voltages with very less distortion but also decrease the dv/dt stresses and electromagnetic compatibility (EMC) problems are also decreases. It can operate at both fundamental and higher switching frequencies.

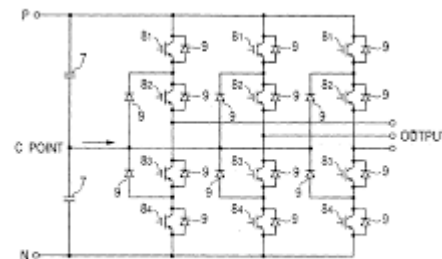


Fig.4 Five level diode clamped inverter

Three-phase five-level diode clamped inverter uses a capacitor in series to divide the dc bus voltage into set of voltage levels. Three-phase five-level diode clamped inverter based UPQC results are carried out by MATLAB/SIMULINK software and compared its results. Therefore, total harmonic distortion of three-phase five-level diode clamped inverter based UPQC reduces are listed compared to proposed UPQC topology

Table 2: THD Comparison Table

Source currents	Conventional (%)	Proposed (%)	Inverter based UPQC(%)
$i_{sa}$	2.72	1.68	0.16
$i_{sb}$	2.72	1.36	0.06
$i_{sc}$	2.73	1.21	0.23

Three-phase Five-level diode clamped Inverter has several advantages. Some of them are given below.

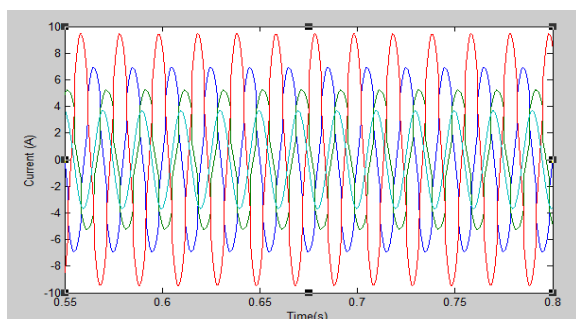
- (a)The THD decreases with the increase in number of levels.
- (b)For all the phases,common dc bus is used.
- (c)Flow of reactive power is controlled.
- (d)Control scheme is quite simple.

### 7. SIMULATION RESULTS

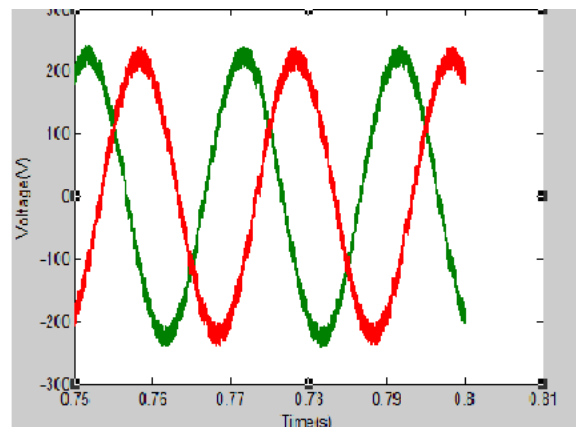
Simulation results was carried by using Simulink/MATLAB software. The simulation results for both modified proposed and conventional topologies are discussed in this section.

#### 7.1 Before compensation

Fig.4(a) shows the load currents are unbalanced and distorted and also fig.4(b) shows the terminal voltages are unbalanced and distorted because these load currents flow into the feeder impedance.



(a)

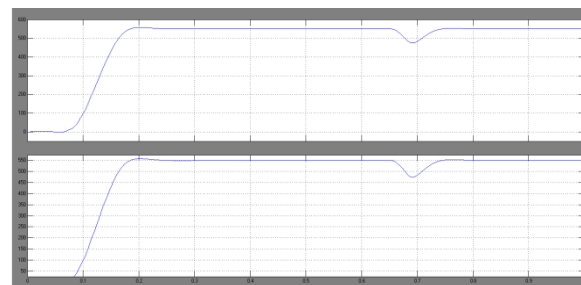


(b)

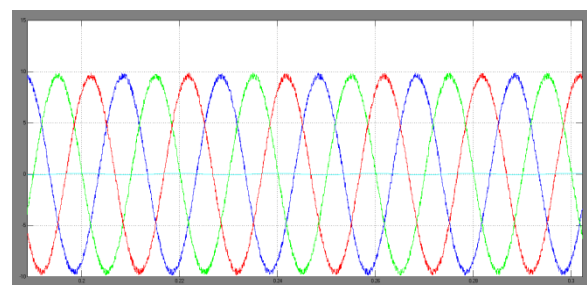
Fig.4.Simulation results before compensation(a)Load currents (b)Terminal voltages

#### 7.2 Conventional Topology

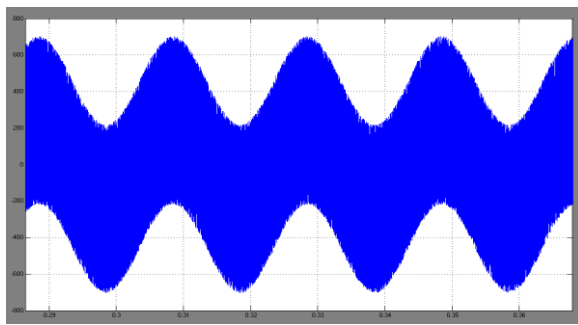
Simulation results of the UPQC of conventional topology is shown in fig.5.The dc-link voltages across the capacitors is shown in fig.5(a).After compensation, the source currents are balanced and sinusoidal as shown in fig.5(b).Fig.5(c) shows the voltage across the interfacing inductor in phase-a. The three-phase shunt compensator currents are shown in fig.5(d).The compensation performance of the series active filter is shown in fig.5(e).After compensation, the load voltages and DVR voltages are shown in same figure.



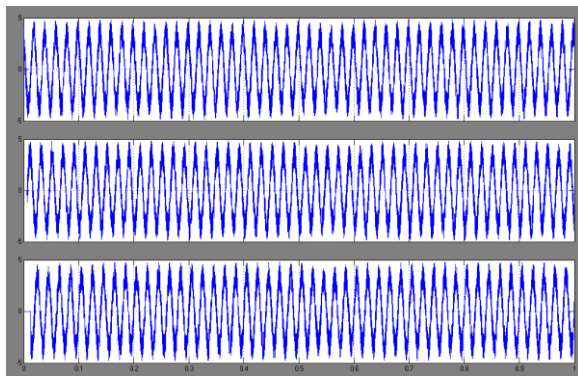
(a)



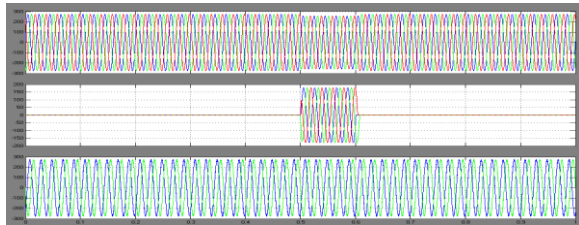
(b)



(c)



(d)

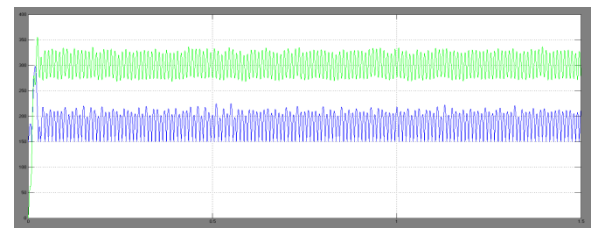


(e)

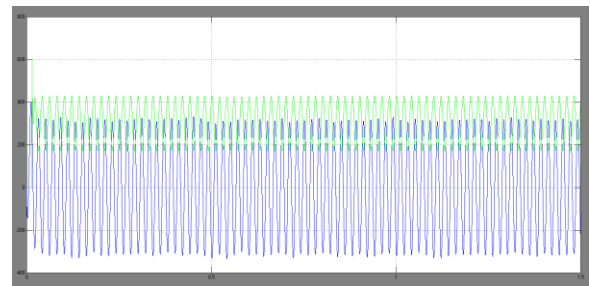
Fig.5.Simulation results using conventional topology.(a)DC capacitor voltages. (b)Source currents after compensation. (c)Voltage across the interfacing inductor in phase-a of the shunt active filter.(d)Shunt active filter currents.(e)Terminal voltages with sag, DVR-injected voltages and load voltages after compensation.

### 7.3 Modified Topology

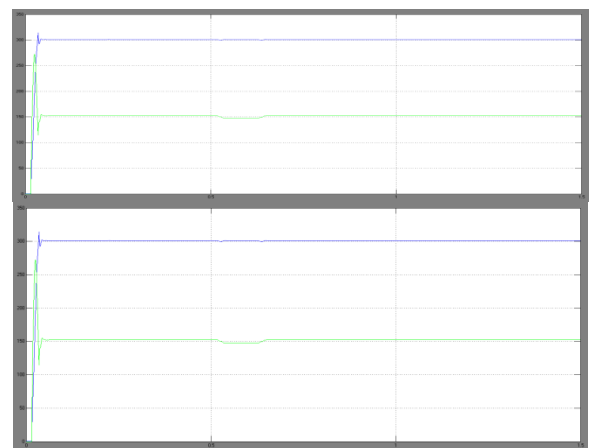
The simulation results of modified topology is shown in fig.6 and 7.The phase-a load voltage and the voltage across the series capacitor in phase-a are shown in fig.6(a).Fig.6(b) shows the inverter output voltage in leg-a.Fig.6(c) shows both the voltage across the series capacitor and a the inverter output voltage for rms value of the fundamental and the dc components.



(a)



(b)

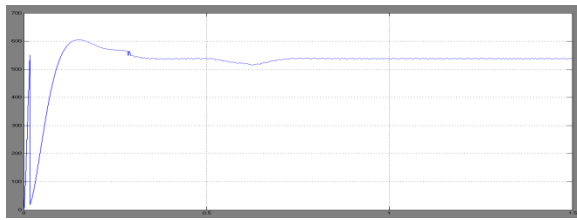


(c)

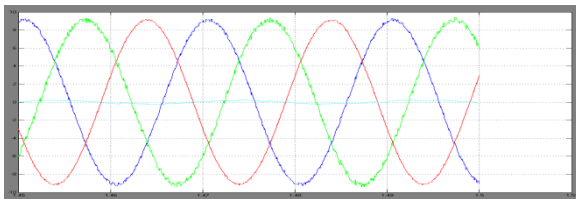
Fig.6.Simulation results with modified topology.(a)Voltage across series capacitor and load voltage in phase-a.(b)Inverter output voltage in leg-a of shunt active filter.(c)DC and fundamental values of voltage across series capacitor and inverter output voltage.

The dc bus voltage is shown in fig.7(a).Using modified topology, after compensation the source currents are shown in fig.7(b).Fig.7(c) shows the voltage across the inductor.Fig.7(d) shows the shunt compensation currents.

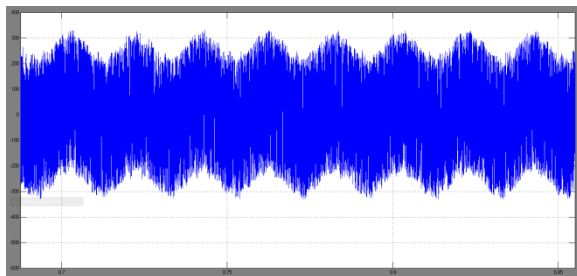
The compensation performance of the series active filter is shown in fig.7(e).After compensation, the load voltages and DVR voltages are shown in same figure.



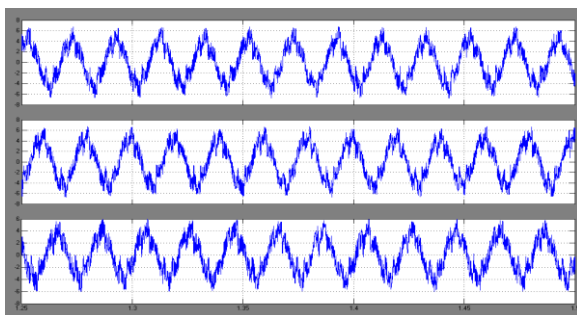
(a)



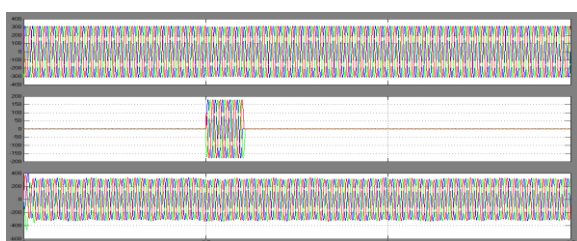
(b)



(c)



(d)



(e)

Fig.7.Simulation results using modified topology.(a)DC capacitor voltages.(b)Source currents after compensation.(c)Voltage across the interfacing inductor in phase-a of the shunt active filter.(d)Shunt active filter currents.(e)Terminal voltages with sag, DVR injected voltages and load voltages after compensation.

## 8. CONCLUSION

In this paper ,a modified Unified Power Quality Conditioner topology for three-phase four-wire system reduces the power quality issues and total harmonic distortion and improves the power quality performance.It has the ability to compensate the load at lower dc-link voltages.The design parameters for shunt and series active filters are explained in this paper.Compared to the conventional UPQC topology, the modified topology has less total harmonic distortion in load voltages and source currents,less average switching frequency. The proposed UPQC topology gives the advantages of both the four leg topology and the conventional neutral clamped topology. Finally, the three phase five level clamped inverter is used to mitigate the THD and improves the power quality of the system.

## 9. REFERENCES

- [1] M. Bollen, *Understanding Power Quality Problems: Voltage Sags and Interruptions*. New York: IEEE Press, 1999.
- [2] S. V. R. Kumar and S. S. Nagaraju, "Simulation of DSTATCOM and DVR in power systems," *ARPN J. Eng. Appl. Sci.*, vol. 2, no. 3, pp. 7-13, Jun. 2007.
- [3] B. T. Ooi, J. C. Salmon, J. W. Dixon, and A. B. Kulkarni, "A three phase controlled-current PWM converter with leading power factor," *IEEE Trans. Ind. Appl.*, vol. IA-23, no. 1, pp. 78-84, Jan. 1987.
- [4] Y. Ye, M. Kazerani, and V. Quintana, "Modeling, control and implementation of three-phase PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 857-864, May 2003.
- [5] R. Gupta, A. Ghosh, and A. Joshi, "Multiband hysteresis modulation and switching characterization for sliding-mode-controlled cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2344-2353, Jul. 2010.
- [6] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768-2775, Aug. 2010.
- [7] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-



controlled systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1047–1058, Mar. 2008.

[8] B. Singh and J. Solanki, "Load compensation for diesel generator-based isolated generation system employing DSTATCOM," *IEEE Trans. Ind. Electron.*, vol. 47, no. 1, pp. 238–244, Jan./Feb. 2011.

[9] R. Gupta, A. Ghosh, and A. Joshi, "Characteristic analysis for multisampled digital implementation of fixed-switching-frequency closedloop modulation of voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2382–2392, Jul. 2009.

[10] B. Singh and J. Solanki, "A comparison of control algorithms for DSTATCOM," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2738–2745, Jul. 2009.

[11] S. Rahmani, N. Mendalek, and K. Al-Haddad, "Experimental design a nonlinear control technique for three-phase shunt active power filter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 10, pp. 3364–3375, Oct. 2010.

[12] V. Corasaniti, M. Barbieri, P. Arnera, and M. Valla, "Hybrid active filter for reactive and harmonics compensation in a distribution network," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 670–677, Mar. 2009.

[13] M. Milane Montero, E. Romero-Cadaval, and F. Barrero-Gonzalez, "Hybrid multi converter conditioner topology for high-power applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2283–2292, Jun. 2011.

[14] J. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR)

at medium voltage level," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 806–813, May 2004.

[15] Y. W. Li, P. C. Loh, F. Blaabjerg, and D. Vilathgamuwa, "Investigation and improvement of transient response of DVR at medium voltage level," *IEEE Trans. Ind. Appl.*, vol. 43, no. 5, pp. 1309–1319, Sep./Oct. 2007.

[16] Y. W. Li, D. Mahinda Vilathgamuwa, F. Blaabjerg, and P. C. Loh, "A robust control scheme for medium-voltage-level DVR implementation," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2249–2261, Aug. 2007.

[17] J. Barros and J. Silva, "Multilevel optimal predictive dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2747–2760, Aug. 2010.

[18] D. Vilathgamuwa, H. Wijekoon, and S. Choi, "A novel technique to compensate voltage sags in multilined distribution system—The interline dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1603–1611, Oct. 2006.

[19] M. Kesler and E. Ozdemir, "Synchronous-reference-frame-based control method for UPQC under unbalanced and distorted load conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3967–3975, Sep. 2011.

[20] K. H. Kwan, Y. C. Chu, and P. L. So, "Model-based *Hinf* control of a unified power quality conditioner," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2493–2504, Jul. 2009.