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Digital PLL Architecture

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Abstract - *ADPLL is contributing vital role in advancement in electronics and digital communication since 1980. Design of ADPLL techniques has made ADPLL very important. ADPLL is still continuing to give better and better results. In the era of modern world ADPLL has great contribution in digital communication systems. This paper gives basic details of an ADPLL. It provides summary of the basic ADPLL principle applicable to electronics and digital communication. It also reports all components of ADPLL and distinguish among them.*

***Key Words*: DCO, ADPLL, loop filter, phase detector, feedback.**

1. INTRODUCTION

The PLL is a self-correcting control system in which two signal compares each other, i.e. input signal and feedback signal. There are four types of PLL 1.linear PLL 2. Digital phase locked loop 3. All digital phase locked loop 4. Software PLL (SPLL). ADPLL takes input as only digital signals. There are so many advantage of the ADPLL due to digital signal as input signal. In this paper different
Applications and importance of ADPLL is discussed [1]-[7].

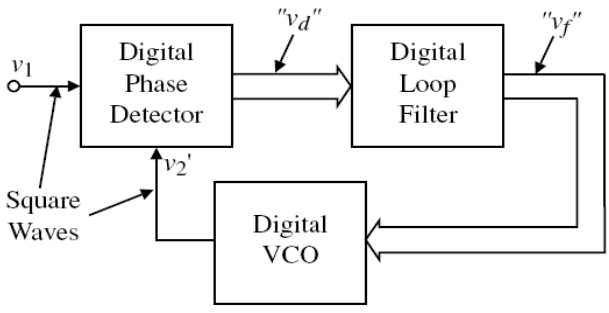

Fig. 1. General block diagram of ADPLL

In the very beginning of all digital phase-locked loops started in 1980 [8]. In the 21'st century, researchers has developed a newly designed digitally controlled oscillator (DCO) to obtain good phase and frequency error. In 2005's, a frequency modulated system based on ADPLL was proposed [2] .In 2006's edge triggered D flip-flop as phase detector was proposed [3]. This design reduced 33% of power dissipation. In 2008 digital FM demodulator was proposed [4] it was designed by VHDL code. In 2009 frequency modulated modem was implemented on field programmable gate array [5] in 2010 a field programmable array based linear All DPLL was proposed. This ADDPLL used field programmable gate array for implementation [6] .Recently an all-digital phase-locked loops (ADPLL) having a fault detection of the input reference signal was modeled in Verilog hardware descriptive language (HDL) [7].

2. ADPLL DESIGN

2.1 Block Diagram

Block diagram contains digital blocks. It uses controlled negative feedback loop. It takes digital signal only. The signal may be single or combination of parallel digital signals. Structure of ADPLL consists three blocks: 1.Phase Detector 2.Loop Filter and 3.Digitaly Controlled Oscillator. Fig. 1 gives basic structure of an All DPLL. The basic aim of the ADPLL is to interlace the phase of input signal v1 and output signal v2' and also the frequency. To reduce the signal error difference among two signals phase detector (PD) is used. For removing noise loop filter is used. At the end the digitally-controlled oscillator (DCO) gets the signals from loop filter which the output signal and makes closer to the input signal. To realize an All DPLL, existing elements must be digital circuits.

2.2 Phase Detector

It is also called as phase compactor. It compares between input signal and DCO output signal. Output signal depends upon the phase error. Output signal contains two types of signal components, low frequency and higher frequency component. Some of the phase detectors are explained below.
1) EX OR gate phase detector
It uses an EX OR logic gate. It compares the reference and DCO signal.

Fig. 2. XOR gate phase detector

Disadvantages of this phase detector are it has phase limitation [-90, +90] degrees and it does not sense edges signal. Fig. 3 shows the "locked" state [8], [11], [13].

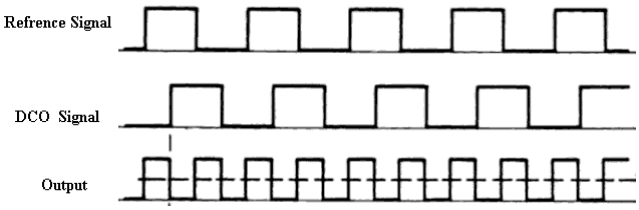

Fig. 3. Waveforms of XOR gate phase detector

2) Edge triggered JK flip-flop PD
It contains a JK flip flop. The phase limitation of this is -180 degrees to +180 degrees. Waveform is shown below [8]-[13].
3) Flip-flop counter phase detector
This phase detector contains a counter and a flip flop, as shown in Fig. 6. Flip-flop Counter phase detector compares reference signal and the DCO output signal. In this case flip flop input S takes input signal and R takes DCO output signal. Output of flip flop is high i.e.1 when there is error among set and reset inputs. Q enables the counter. FF input S resets counter. Output of counter depends upon the phase error. Waveform of this is shown below.

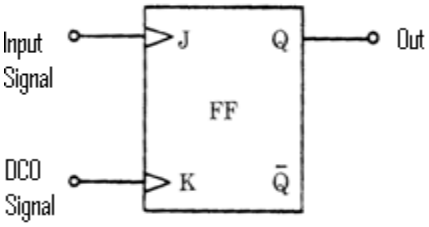

Fig. 4. JK flip-flop phase detector

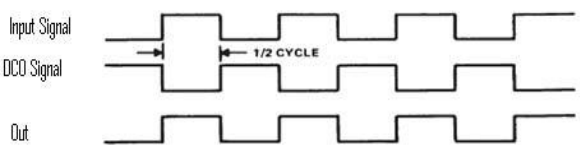

Fig. 5. Waveforms of JK flip-flop phase detector

2.3 Loop Filter

Basically it is an integrator. Examples of loop filters are discussed below.
1) UP/down counter loop filter
It is the very simplest loop filter. It is always operate in conjunction with EX OR or J K FF PD. For getting clock and direction signal a pulse forming circuit is used. Up / down Counter is incremented on each UP pulses and it is decremented on each down signals .So its work like an integrator [8], [11].
2) K counter loop filter
K counter loop filter is important loop filter .It always works with J K FF or EX OR FF phase detector. It is having two counters .Both are individual .One is called up counter and other is down counter .But both counts in upward direction. Counter has modulus k. So counter contents has range from 0 to k-1.Counter clock frequency is N times multiple of center frequency. M has typical values of 8, 16, 32....Down counter is enabled when DN/UP has logic level high and up counter is enabled when this logic level low value. When contents exceed k-1 both counters resets. "Carry" is MSB of the Up counter .The "borrow" signal is MSB of the Down counter. When Up-counter stored data ≥ k/2 "carry" is high .When down counter stored data≥ k/2 "borrow" is high. Frequency of digital control oscillator is controlled by positive edges of the signal [8], [11], [13].

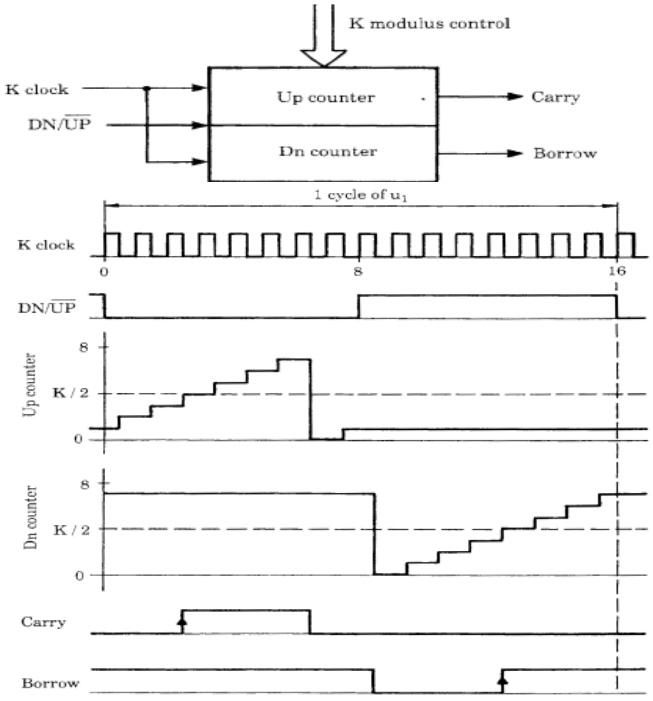

Fig. 6. K Counter Loop Filter. (a)Block Diagram.
(b) Corresponding waveforms.

2.4 Digitally Controlled Oscillators

Digitally Controlled oscillator is nothing but a modified oscillator .Depending upon output signal of the loop filter they change their frequency. Some of digitally Controlled oscillators are explained below.

1) Divide by N counter digitally Controlled oscillator

A simple ÷N counter works as digitally Controlled oscillator. IT operates at very high frequency signal. Divide by N counter produces N bit parallel output [8], [11]. Drawback of it is we can't design jitter

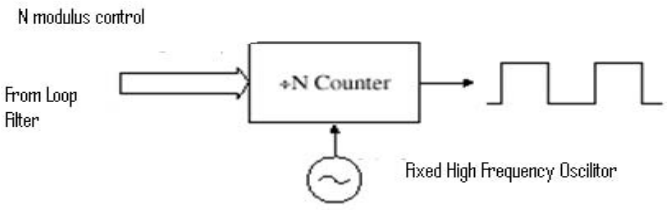

Fig. 7. ÷N Counter DCO

3. APPLICATIONS OF ADPLL

ADPLL with is developed for digital communications [8], for example, FSK decoder. ADPLL can be used for wide-band frequency tracking and noise reduction [12]. PLL heating control system was replaced by ADPLL in 2009 [13]. FM demodulation on ADPLL circuit was proposed [14]. For mobile phones applications ADPLL is developed [15]. ADPLL is used in high-speed clock generation [16], [17]. There are no of ADPLL developed for frequency synthesizers [17]-[19]. In communication systems like wireless ADPLL is very helpful [20]. ADPLL is used in Clock recovery circuit and in frequency synthesizers [21]-[26].

4. CONCLUSIONS

General block diagram of an ADPLL has been discussed. Possible different type's implementations of all the blocks of ADPLL have been described. Comparison between all the blocks have been discussed in detail. Typical applications of the ADPLL is summarized. ADPLL block implementations have been presented.

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