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A Review on DMC for Multiple Cell Upset Correction in Semiconductor Memories

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Abstract - *An important issue in data storage is semiconductor memories is transient multiple cells upsets (MCUs) when exposed to the radiation environment. There are many available packaging techniques which defend the memory data from radiations and transients. A particular packaging provides data safety from a limited variation of radiations. With the increasing demand in the application of wireless communication a very wide range of radiations. Subsequently, some additional data protection techniques like Error Correction Codes (ECCs) are always chosen for authenticating the data before it is processed. These techniques use encoded data to be stored in memories. A review on Decimal Matrix Code (DMC) based memory data error detection and correction is presented in this paper.*

Key Words: Matrix Data Representation, Decimal Addition, Error Correction Codes, Hardware Memory, Multiple Cell Upsets.

1.INTRODUCTION

The demand of scaling down in CMOS technology to deep nano-scale and that are exposed to space environment radiations are the cause for an increase in the soft error rate in memory cells. The charge stored in semiconductor memory as data are affected by the energy radiations that have ionizing characteristics. These energy particles introduce soft error in the memory. This phenomenon is represented with the help of memory block in fig. 1. In this figure M0 - M7 is the Memory Data Register that stores 8-bit data (eg, 11001100). When this memory data is exposed to the Energy Radiation, The affected memory data gets changed. In the example the radiations affect the third-bit (M2) and the fifth-bit (M4). So the data inside the memory becomes 11100100. This example shows a major concern about memory reliability against radiation caused errors. These errors can be single-bit or multiple-bit. In order to tolerant such faults in the memory up to the maximum possible level, many researchers recommend some error correction codes (ECCs).

A simple block diagram of the fault tolerant architecture based memory implementation is shown in fig. 2. For correcting the error, a block is needed to encode the data that is to be stored in the memory and this data is first used to generate redundant bits. Memory interface is used to store the data bits and the redundant bits in the memory. These redundant bits are used to detect and correct the errors in the memory data when the data is read from the memory. Some of the most reliable codes that are proposed by the researchers include Reed-Solomon (RS) code Bose-Choudhary-Hocquenghem (BCH) code and Punctured Difference Set (PDS) code. These are the codes that have been used to deal with multiple-bit error correction in memory. The arrangement of memory bits in the memory architecture uses the concept of interleaving. In interleaving, the rearrangement of the cells in the physical arrangement breaks the bits into different physical words.

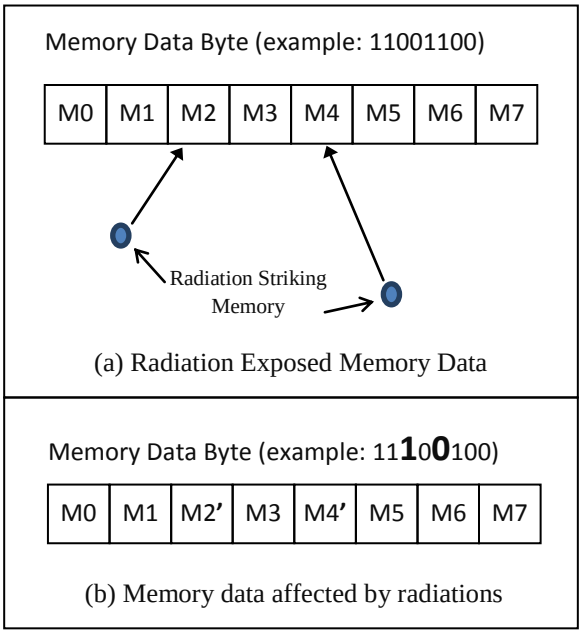

Fig. 1 Soft Error caused in Semiconductor Memory due to exposure to Energy Radiation

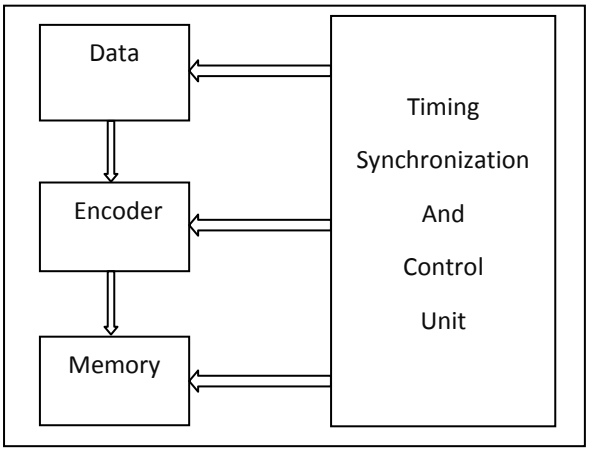

Fig. 2 A simple data encoder block

A 2-D matrix architecture based encoding is a code for efficiently correct the MCUs per word. In this code the word is divided into multiple rows and columns. Further, Hamming code or Parity code can be used to protect the bits per rows and per columns. Here, the bits per row are protected by Hamming Code and the bits per column are protected by parity code. The decoding of data to detect and correct error by 2-D matrix coding technique has a lower delay overhead as compared to other techniques. To provide improved memory reliability the matrix code uses the concept of divide-symbol. Decimal integer addition (decimal algorithm) on the divided symbols of binary code is performed on the matrix coded data symbols. Logic comparator unit is involved to detect the errors and finally error corrector logic block is used to locate and correct the error. The rest of this paper is arranged as follows: the work published by some recent scholars is presented in section-II. Section III presents the conclusion of the review presented in this paper. In the last section the referenced papers are listed.

2. LITERATURE REVIEW

Reference [1] proposes a novel per-word DMC to assure the reliability of memory. To detect errors the proposed security code utilized decimal algorithm as a result of which more errors were detected and corrected. The proposed result shows that the scheme has a superior protection level against large MCUs in memory. An adequate level of immunity is provided by the proposed decimal error detection technique for detecting MCUs in CAM as it can be combined with BICS. The work performed in reference [2] presents a relative study of various error correcting codes that define various alternate to prevail over dependability issue of memories. To avoid the occurrence of MCUs several error correction codes (ECCs) are used but their efficiencies are different in terms of delay overheads and the complexity of encoder and decoder architecture. To minimize the area and delay overheads by comparing with the existing techniques like built in current sensor, hamming, matrix codes, etc. the proposed system uses decimal matrix code (DMC). Improvement of the memory consistency is obtained by enhancing error correction capability.

A matrix architecture based decimal correction code is proposed in reference [3]. This work used hamming code encoding for maintaining data integrity. In this work the area overhead is minimized without interrupting the encoding and decoding operations. The design is implemented and analyzed with the help of the encoder-reuse technique (ERT). A 64-bit data arranged 2-D matrix architecture based DMC encoding for memory data protection is implemented in [4]. To save the memories from data corruption complex error correction codes are widely used to protect memory, however higher delay overhead is the problem that is required to be solved in such designs. Hamming codes based matrix codes are commonly and effectively used for memory protection such designs.

Reference [5] proposed a mechanism that uses hamming code for are single error correction-double error detection–triple-adjacent error detection. This work uses the codes resulting From Orthogonal Latin Square Codes for single and double adjacent error correction, double nonadjacent and triple error detection. A novel decimal matrix code in proposed in [6] to assure the reliability of memory against errors. The protection level against large MCUs in memory is better challenged by the proposed algorithm. The proposed decimal error detection technique is an attractive opinion to detect MCUs in CAM because it uses the architecture of BICS to provide an adequate level of protection. Reference [7] presents two Error Correction Codes; Parity Matrix Code (PMC) and Decimal Matrix Code (DMC). The Encoder-Reuse Technique (ERT) is utilized to play down the area overhead of additional circuits without altering the whole encoding and decoding processes. PMC uses hamming algorithm to detect and correct errors, so that more errors can be detected and corrected. A compared to DMC, the PMC requires less area overhead and less number of redundant bits.

Reference [8] presents a work with the implementation of matrix code for error detection and correction in memories. Hamming and parity based architectures are implemented in this work. Error correction upto 2-bits is performed using hamming code. This is further improved by the implementation of decimal matrix code. The area overhead is reduced by implementing encoder reuse technique. Reference [9] presents a decimal algorithm based

implementation of memories for error correction. The result in this work shows that the proposed scheme has a better protection level in opposition to large MCUs in memory. Here the protection of data is achieved by changing Carry Save Adder (CSA). Traditional 2-D repair approach is combined with the proposed technique and the defects are handled by the SEC-DED codes. This method would provide a complete protection against soft errors in semiconductor memories.

Reference [10] propose HMC (Hamming Matrix Code) based design which a hybrid matrix code that offers an improved memory consistency against multiple cell upsets. As compared to the accessible approaches it required less number of redundant bits for data security. The proposed scheme results in a better-quality protection level against large MCUs in memory. The work in reference [11] proposed DMC scheme to assure the reliability of the memory. The projected scheme shows a superior security level against large MCUs in memories. This work shows the only shortcoming of more redundant bits requirement to maintain higher dependability of memory space.

An ERT based DMC implementation is performed in reference [12]. Decimal Algorithm is used in this work to obtain the error detection and correction capability. The Encoder-reuse technique (ERT) based on DMC is used to minimize the area overhead. A 2-D matrix is prepared to set the data bits that are spitted into symbols. DMC encoder performs the decimal operation to compute horizontal redundant bits and vertical redundant bits. After encoding the data, codeword is stored in the memory. In the condition when the radiation affects the memory, the cell upset problem might arise. In this condition, the Decoder is used to solve the data correction. Another DMC based design and implementation is performed in reference [13]. In this method a 128-bit data based Decimal Matrix code implementation is performed for detection and correction of errors in the memories and to maintain memory reliability. This proposed DMC architecture increases the error detection and correction ability, decreases the area, maintain the memory reliability and shows a reduction in redundant bits. The work in reference [14] proposes a security code DMC design that utilizes decimal algorithm to detect more than single-bit errors.

In Reference [15] the proposed Decimal Matrix Code algorithm is designed by performing decimal ex-or and addition/subtraction operation to detect and correct errors in the memory. The proposed design consumed less power by using the implemented concept as compared to the other existing codes. The only drawback of DMC is the requirement of storing comparatively more number of redundant bits. Reference [16] proposed HMC (Hybrid Matrix Code) to assurance the reliability of the memory against radiation generated soft errors. This design also have the same disadvantage of more number of redundant bits. In reference [17] Enhanced protection to memory detection is proposed using DMC design for multiple MCUs. Reference [18] proposed DMC which provides a competent error correction code by which the security of the memory data is improved. The proposed design uses decimal algorithm which acquire integer subtraction and addition that are simple and fast to implement and execute using high speed hardware.

3. CONCLUSIONS

This paper presents a review on the matrix architecture based memory data encoding to detect and correct radiation encountered soft errors. A number of papers are studied under this work to review the existing work. The emerging application of error detection and correction code for memories is the idea behind the study. This idea further need a lot of work to be implemented in the same line as the applications of semiconductor memories is increasing day-by-day along with an increase in the amount of high energy radiations in the environment due to wireless communication.

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