

Study of five level inverter for harmonic elimination

Farha Qureshi¹, Surbhi Shrivastava²

¹ Student, Electrical Engineering Department, W.C.E.M, Maharashtra, India

² Professor, Electrical Engineering Department, W.C.E.M, Maharashtra, India

Abstract -In Multilevel Inverter technology has emerged recently as a very important alternative in the area of high power, high voltage energy control. It came into picture and it has gained more attention in market for various applications like renewable energy systems, industrial motor drives, etc. It can generate stepped waveform by reducing harmonic distortion with increase in the number of voltage level. In this paper, one carrier based PWM technique is proposed i.e. level shifted scheme which can minimize the total harmonic distortion and enhances the output voltage. Level Shifted [LS] Scheme is applied to the Cascade H-bridge multilevel inverter and the complete analysis of THD to three and five levels is done. The simulation is done by MATLAB R2010a version software.

Key Words: %THD, CHB multilevel inverter, carrier-based PWM scheme, MATLAB/Simulink software.

1. INTRODUCTION

The tremendous increase in energy demand led to call of high power converter technology to transmit the power with high accuracy. When dealing with high voltages, conventional inverters produce output voltages of low quality and high harmonic content which affects the equipment performance. So new power converter topologies were invented known as multilevel inverters and gained importance in industry applications because of high power ratings and better harmonic performance suitable for medium and high power applications. The output voltage of multilevel inverters is in form of stepped waveforms and obtained easily without use of transformers which decreases the cost of inverter. Improved quality of waveforms can be obtained by increasing number of steps in the output waveforms and the harmonic content also comes down. Multilevel Inverters are classified into three topologies namely diode clamped, flying capacitor and cascaded type inverters. PWM is a technique in which width of gate pulses are controlled and used for various applications. Different

types of PWM techniques are proposed for multilevel inverters like sinusoidal pulse width modulation, selective harmonic elimination and space vector modulation. SPWM is considered as the best technique among other PWM methods because of various reasons like high power handling capacity, no temperature variation, easy to implement and control. Here SPWM is used for modelling of three level and five level cascaded H-bridge inverter. The design and modelling of three levels and five levels CHB is done in MATLAB/SIMULINK. In this proposed concept uses the IGBT semiconductor switches.

2. CASCADED H-BRIDGE MULTILEVEL INVERTER (CHMLI):

The cascade inverter in the figure 1, can produce a phase voltage with five voltage levels. The resultant inverter phase voltage is $V_{AN} = V_{H1} + V_{H2}$, which is the voltage at the inverter terminal A with respect to the inverter neutral N. The output voltage can be $0, \pm E, \pm 2E$. The voltage levels which correspond to various switching states are summarized in table 1. It can be observed from the table that some voltage levels can be obtained by more than one switching state. These redundancies are common in multilevel inverters. It provides a great flexibility for switching pattern design, especially for space vector modulation schemes. In a general way If H is the number of single-phase H-bridges per phase, the number of levels of the inverter is:

$m = (2H + 1)$ where, H is the number of H-bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter. The total number of active switches (IGBTs) used in the CHB inverters can be calculated by, $N_{sw} = 6(m - 1)$ Where, N_{sw} is total number of switches and m is a voltage level. [1]

Advantages:

1. The multilevel inverter is composed of multiple units of identical H-bridge power cells, which leads to a reduction in manufacturing cost .

Lower voltage THD and dv/dt. The inverter output voltage waveform is formed by several voltage levels with small voltage steps. Compared with a two-level inverter, the CHB multilevel inverter can produce an output voltage with much lower THD and dv/dt.

Disadvantages:

1. Large number of isolated dc supplies- The dc supplies for the CHB inverter are usually obtained from a stiff DC supply employing an expensive phase shifting transformer.
2. High component count- The CHB inverter uses a large number of IGBT modules. A five-level CHB inverter requires 24 IGBTs with the same number of gate drivers.

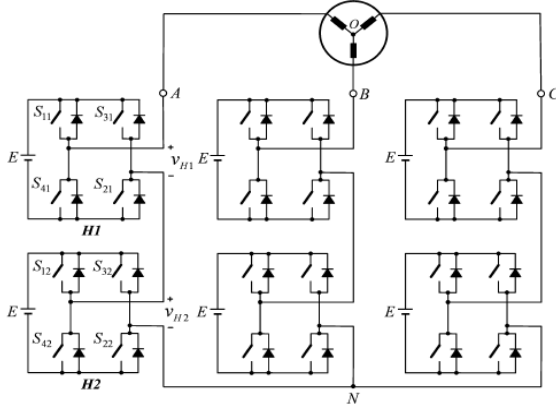


Fig- 1: Five-level cascaded H-bridge inverter

In this diagram, the 24 no. of IGBTs are used and after that get the output 5 level voltage. The output is given to the 3-Phase load like as R-L load taken normally. The pulses are generating by comparing the triangular wave and sinusoidal wave. For 5 level output, the triangular wave are taken N-1. Means 4 triangular waveform required. Which are compare to sinusoidal waveform and pulse are given to the each IGBT.

Table 1

Output voltage VAN	S11	S31	S12	S32	VH1	VH2
2E	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	-E
	0	1	1	0	-E	E
-E	0	1	1	1	-E	0
	0	1	0	0	-E	0
	1	1	0	1	0	-E
	0	0	0	1	0	-E
-2E	0	1	0	1	-E	-E

3. Harmonic Reduction Technique:

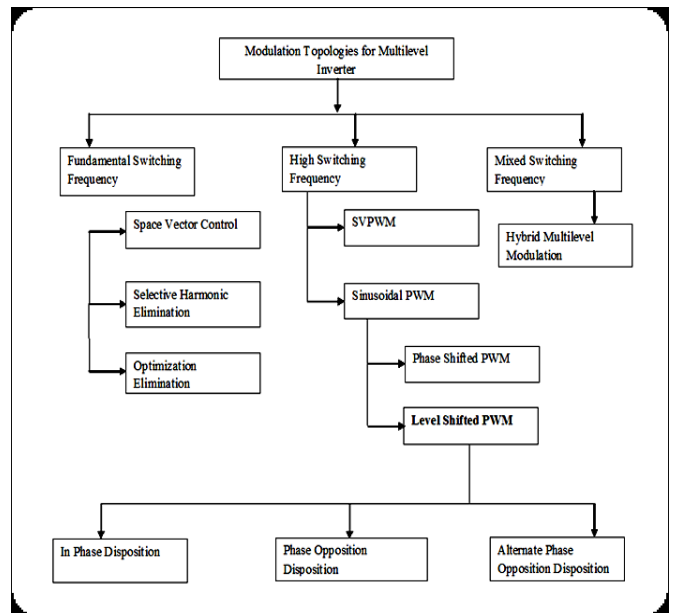


Fig-2: classification of multilevel inverter control techniques

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge inverters. Total harmonics distortion of phase-shifted modulation is much higher than level shifted modulation. Therefore we have considered level-shifted

modulation. An m-level multilevel inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index is given by $mf = f_{cr}/f_m$, which remains the same as that for the phase-shifted modulation scheme whereas the amplitude modulation index is defined as

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}(m-1)} \quad \text{for } 0 \leq m_a \leq 1 \quad \dots(1)$$

where \hat{V}_m is the peak amplitude of the modulating wave v_m and \hat{V}_{cr} is the peak amplitude of each carrier wave. The Level shifted pulse width modulation have three types named as In-phase Disposition (IPD), Phase opposition disposition (POD) and Alternate phase opposition disposition (APOD). [1],[6]

- (a) in-phase disposition (IPD), where all carriers are in phase.[1],[6]
- (b) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition.[1],[6]
- (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. [1],[6]

4 .SIMULATION AND RESULTS:

Table - 2 THD Comparisons of PWM Technique

SR.NO	PWM Technique	No. of levels	% THD
1	IPD	3 Level	36.77 %
2	APOD	3 Level	63.16%
3	POD	3 Level	63.88 %
4	IPD	5 Level	19.20 %
5	APOD	5 Level	28.50 %
6	POD	5 Level	33.43 %

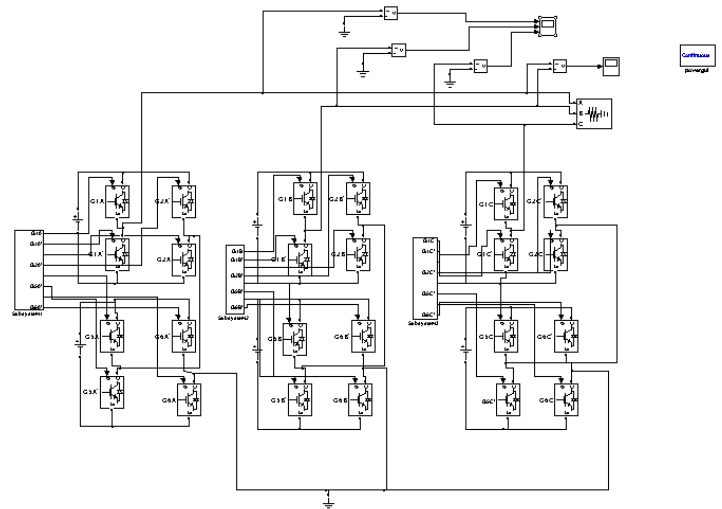


Fig -3: Simulation circuit diagram of 3 phase five level CHB inverter

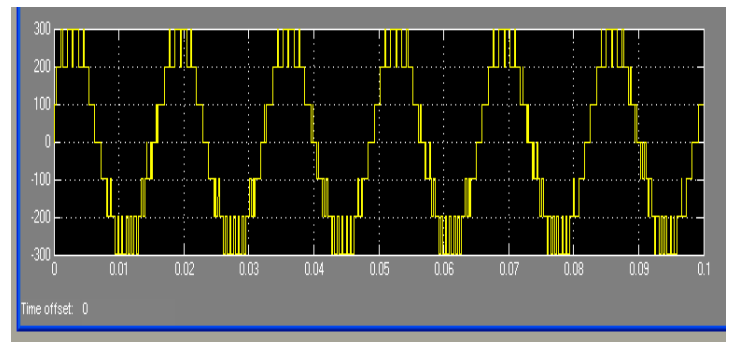


Fig -4: Showing the output voltage of 5level CHB inverter.

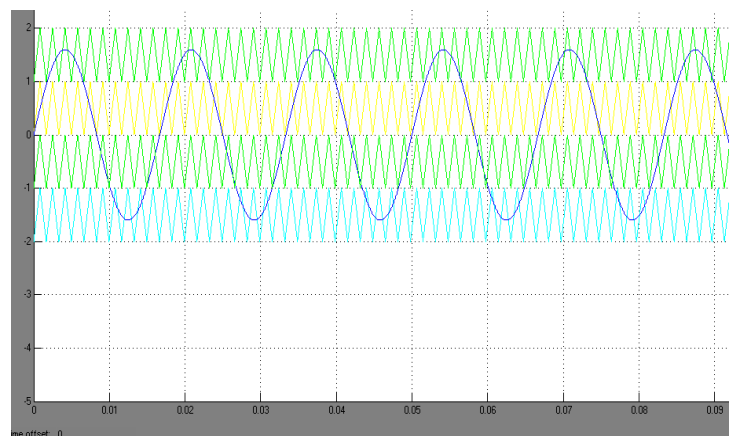


Fig-5: Showing Simulation result of IPD PWM scheme for 5level CHB inverter

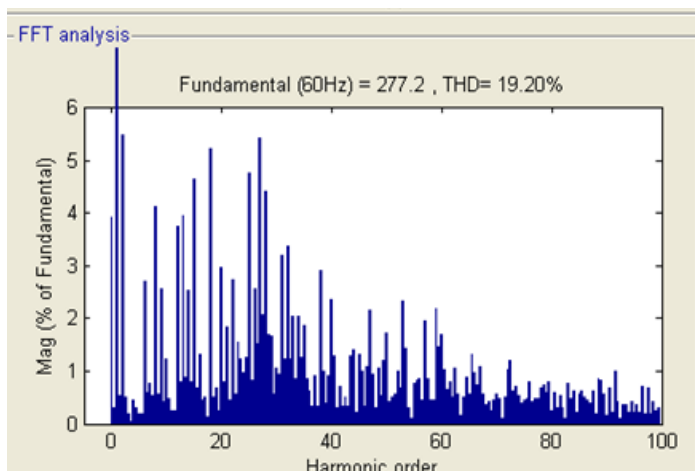


Fig -6 : Showing THD Analysis of IPD for 5level CHB inverter

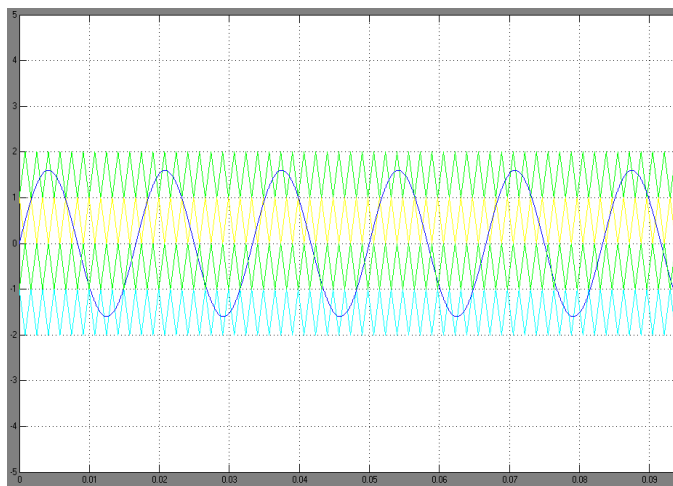


Fig -7 : Showing Simulation result of APOD PWM scheme for 5level CHB inverter

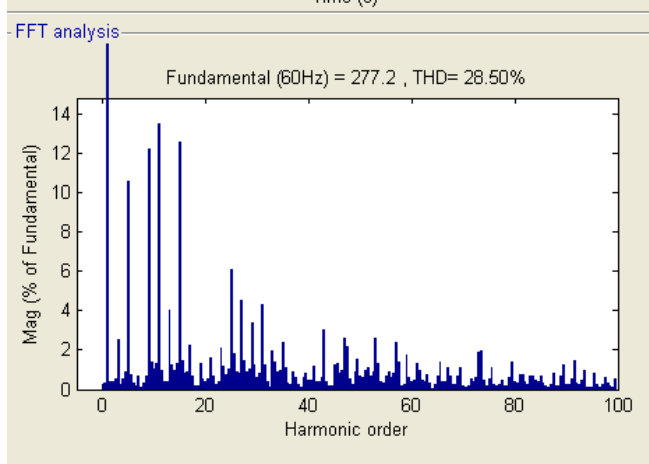


Fig -8: Showing THD Analysis of APOD for 5level CHB inverter

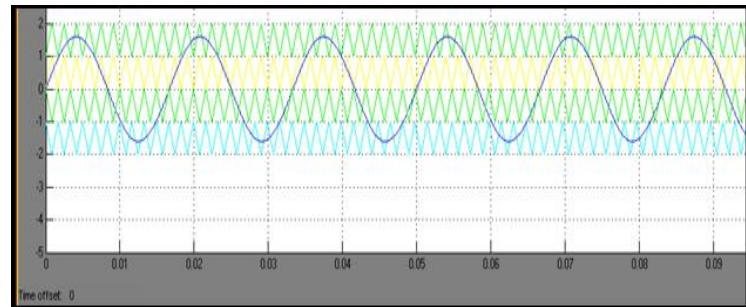


Fig -9: Showing Simulation result of POD PWM scheme for 5level CHB inverter

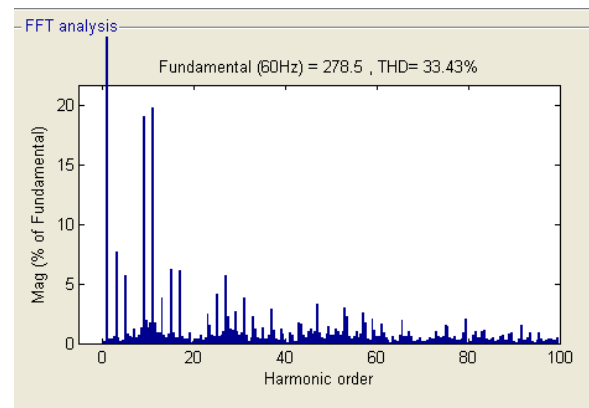


Fig -10: Showing THD Analysis of POD for 5level CHB inverter

Similarly simulation result of 3phase 3 level CHB inverter is given below.

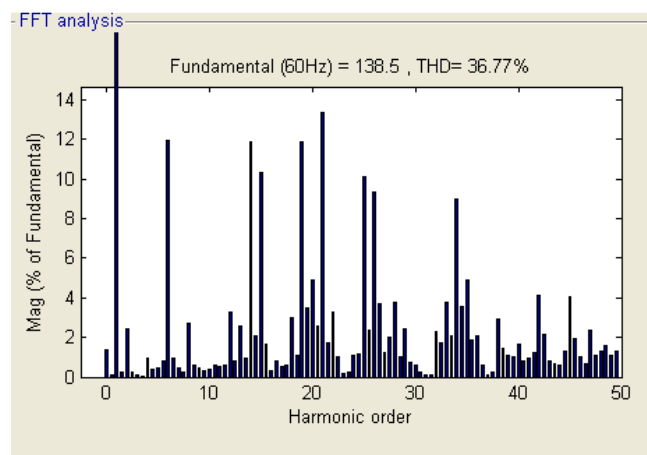


Fig -11: Showing THD Analysis of IPD for 3level CHB inverter

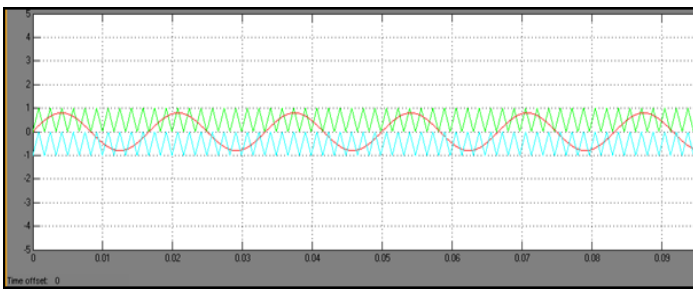


Fig-12:Showing Simulation result of IPD PWM scheme for 3level CHB inverter

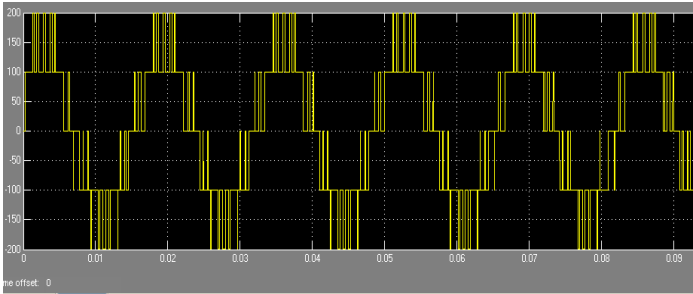


Fig -13: Showing the output voltage of 3level CHB inverter.

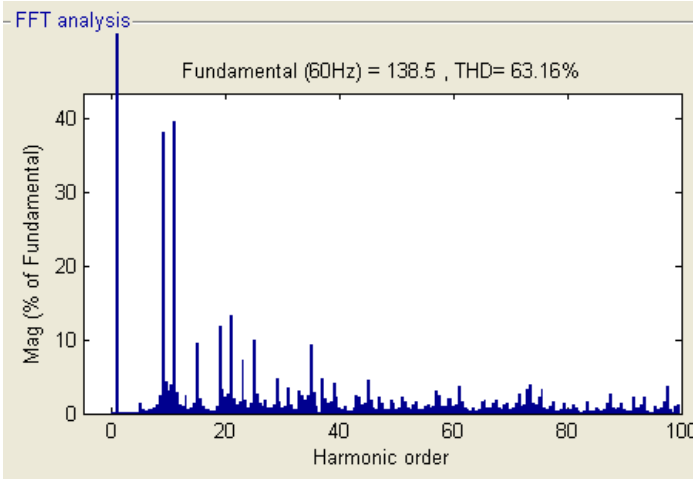


Fig-13 Showing THD Analysis of APOD for 3level CHB inverter

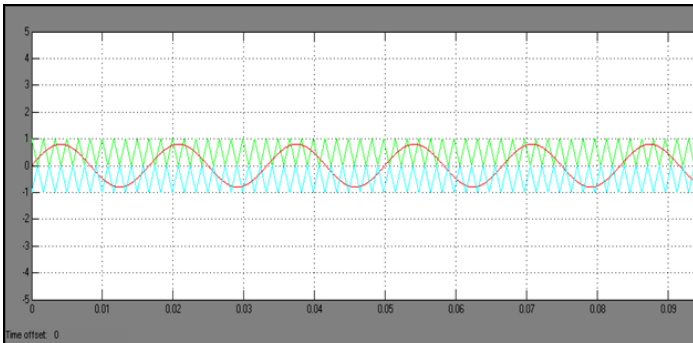


Fig-14: Simulation result of APOD PWM scheme for 3level CHB inverter

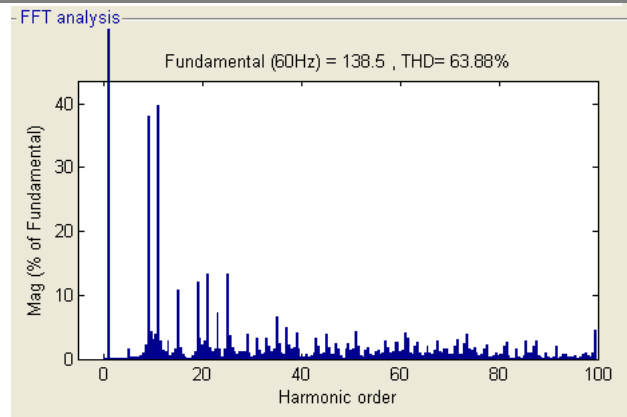


Fig-15: Showing THD Analysis of POD for 3level CHB inverter

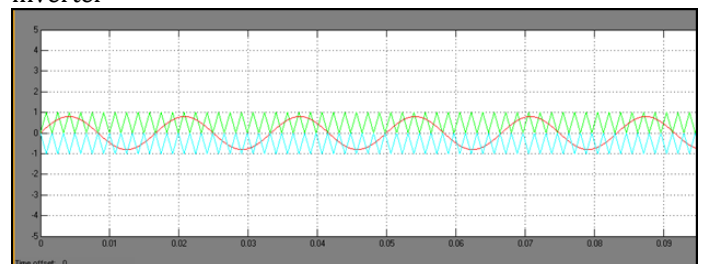


Fig-16: Showing Simulation result of POD PWM scheme for 3level CHB inverter

5. CONCLUSIONS

Multilevel inverter are very suitable for PV generation. A bridge cell with PWM control is a very promising solution not only for having medium and high voltage but for improving the quality of the voltage i.e. reduction of THD. In this paper we have discussed the CHB inverter topology using IPD, APOD and POD and they are compared. Further it is observed that IPD is better and yields less THD as compared to APOD and POD in 3 level and 5 level CHB inverter. Simulation results show that when we increase the number of levels THD gets reduced in the output voltage waveform.

ACKNOWLEDGEMENT

The authors thank Prof. Surbhi Shrivastava for their support.

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BIOGRAPHIES



Farha Qureshi was born in Nagpur, India. She received the BE. Degree in electrical engineering from and the Rashtrasant Tukdujimaharaj University Nagpur, India, in 2011 and presently M.Tech pursuing. Her fields of interest are power electronics, power systems, and renewable energy



Surbhi Shrivastava was born in Nagpur, India, . She received the BE. Degree in electrical engineering from CSVTU BHILAI University India, in 2010 and received M.Tech in Electrical Devices and power system engineering from CSVTU BHILAI University India, in 2014. Her fields of interest are power electronic s and power systems.