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Performance Analysis of Two-Stage Op Amp using different BIST Techniques

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Abstract - *The IC fabrication technology is growing rapidly in present days. As a result, millions of transistors can be manufactured on a single chip. The high integration density and increasing complexity limits the accessibility and observability to the internal components because of limited I/O pins. Thus, the traditional off-chip testing techniques are more difficult and challenging for IC testing. Particularly, analog part testing is more difficult than digital. So, more care has to be taken on analog part. This paper presents two types of BIST techniques for testing two stage operational amplifier. Oscillation Testing Methodology(OTM) and Stable Output Value(SOV) based BIST Techniques are used to increase the fault coverage.OTM converts the CUT into oscillator and does not need any modification in the circuit whereas the SOV BIST Technique converts Op Amp into voltage follower and also uses stimulus generator and SOV Checker .Fault coverage of OTM is more than SOV.*

Key Words: – Oscillation based Testing Methodology(OTM), Stable Output Value based BIST(SOV), Two Stage Op Amp, Step Signal Generator, SOV Checker.

1.INTRODUCTION

The need of electronic components is increasing rapidly. Especially there is a great demand for digital devices compare to analog devices. The testing of digital, analog and mixed signal devices is difficult in terms of area, time and power. The testing of analog and/or mixed signal devices is much more difficult compare to digital devices. There are various testing methodologies in this regard. Specification based testing methodology encounters difficulty due to circuit complexity and timing constraints. So, Fault based techniques are used to decrease this complexity.

2. ANALOG AND MIXED SIGNAL BIST TECHNIQUES

Oscillation based Testing Methodology (OTM) was explained in paper[1] and [2] .This method converts the CUT into an Oscillator and the correctness of the circuit is determined by measuring deviation in Natural frequency of oscillation. Paper [3] and [4] explains about the transient response analysis based technique. Here Op Amp is converted into voltage follower circuit . The overshoot and slew rate deviation are considered as parameters for testing. In [5] an AC and DC compacted techniques were proposed. In this technique the amplitude and offset voltages were taken as parameters to detect faults. However this in infeasible as the sinusoidal wave generation circuit involves more complexity. Paper [6] explains about IDDQ testing technique in which power supply in monitored to find change in current due to faults. Use of current sensor results in Performance degradation. Paper [7] explains about converters. The analog devices such as ADC(analog to digital converter) and DAC(digital to analog converter) are very important mixed signal circuits. These converters are majorly used in any electronic devices. Converters contains many sub-circuits like sample and hold circuits, Quantizers , low pass filters, amplifiers etc. BIST Techniques are applied to individual sub-circuits and tested. Fault free subcircuits are combined and tested for proper functionality of the converters. One BIST circuit can be shared by many sub-circuits. A fault-free sub-circuit can be used as BIST circuit for another sub-circuit. Thus the complexity and area of the circuit decreased. A high level test bus or controller used to control the whole testing procedure. Test Controller is generated by the digital Block. Paper[8] explains about the use of DSP for BIST Technique. For Mixed signal devices such as ADC and DAC ,a BIST technique developed which uses a Digital Signal Processor(DSP).A DSP is programmed such that it acts as stimulus generator, Response Analyzer and also Test controller. This technique not only improves testability but also increases device calibration. This technique uses a Sigma-Delta Testing and Polynomial fitting algorithm. Oversampled Sigma-Delta modulation is used for test signal generation and analyzing the response for high accuracy. A multiple bit Sigma-Delta Encoder software is used to avoid DAC imperfections. This technique uses analog sine signals as test stimulus and digital sine signals as reference signals. The important parameters considered here are differential nonlinearity, integral nonlinearity, gain and offset. Nonlinearity errors are detected by Polynomial

fitting algorithm and reduced by polynomial. Paper[9] explains about Realistic Fault Analysis using nets. Major faults occurs in IC manufacturing process are Spot defects which occurs during Lithographic process. Spot defect may be an extra material or missing material on the chip. These defects results in functional failure of the chip. Single stuck-at fault models analysis is one of the methods used to detect spot defects. But this method does not detect all the bridging faults, it may detect only 50% of the faults. So, the realistic fault analysis using nets plays vital role in this regard. This method not only deals with stuck-at 0/1 but also it accounts the information about technology, processing defect statistics ,layout data. This is considered as the more accurate method resulting high testability and more circuit yield. Two types of yield simulators used. Monte-Carlo simulator called VLASTIC and RYE is an Analytical based approach used to find probability of catastrophic faults. In Real Fault Analysis method, the faults caused by spot defects are analyzed and extracted net by net and it is applied to the entire layout to find all faults. It was implemented on HP750 workstation. Its was demonstrated on all layouts of iscas85 benchmarks, and also layouts having about 28000 transistors. This was much faster than the other analysis methods. In this Paper two BIST Techniques (1)OTM and (2)SOV based BIST Techniques are implemented.

3.OSCILLATION BASED TESTING METHODOLOGY

A Two stage Operational Amplifier is shown in figure 1.This Op Amp is converted into an Oscillator by giving negative feedback. Negative feedback is given through R & C components.

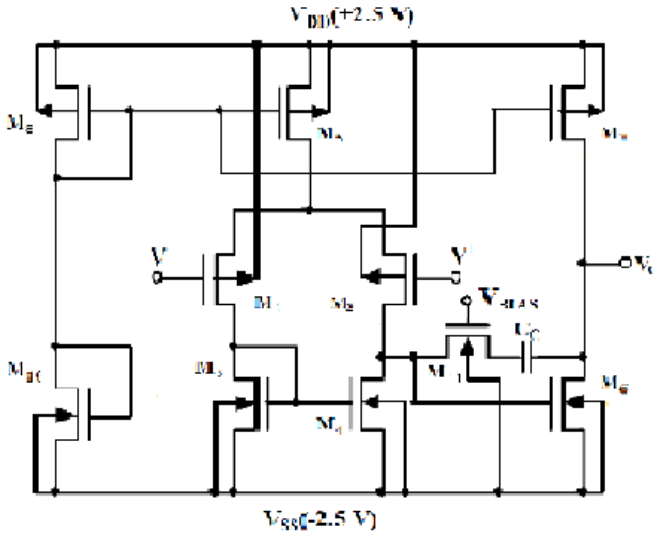

Fig-1: Two Stage Op Amp

The converted Oscillator is shown in the figure 2 below. In this no input is given to the input terminals, only feedback is given. The RC delay in the feedback network causes oscillations. The overall gain and phase results in oscillations. The feedback components can be adjusted to get self-sustained oscillations. The natural frequency of oscillations are obtained by fault-free circuit or by Monte-carlo simulation. For every fault injected, the frequency of oscillation has to be measured. If it is +/- 10% close to natural oscillation frequency, then the circuit is considered to be fault-free otherwise faulty.

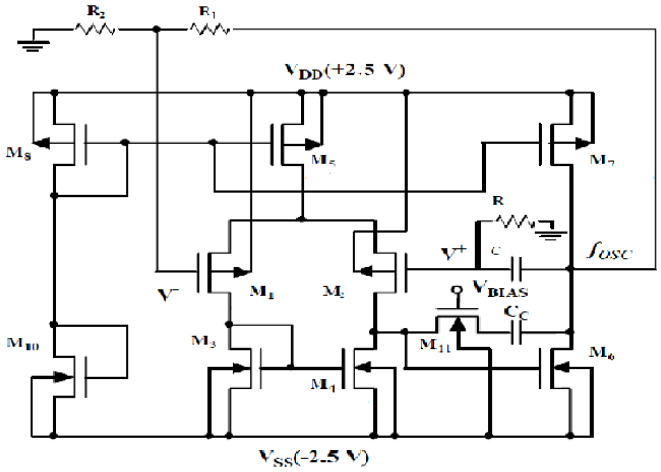

Fig-2: Converted Oscillator

The values of transistors, resistors and capacitors are given in Table 1.

TABLE-1:ELEMENT PARAMETERS OF OP AMP OSCILLATOR

Elements	Size(Unit)	Elements	Size(Unit)
M8,M5	50/1.345(um)	M6	50/2.275(um)
M1,M2	24.8/3.2(um)	R1	3K
M3,M4	17.6/3.2(um)	R2	500K
M10	5.2/10.4(um)	R	20K
M11	8.8/7.2 (um)	C	100pF
M7	50/0.68(um)	Cc	2pF

4. STABLE OUTPUT VALUE(SOV) BASED BIST TECHNIQUE

The proposed SOV BIST architecture is shown in figure 3.This Technique consists of a step signal generator, an op amp and a SOV checker. At test mode a negative or positive step signal is generated, and it is given as input to the op amp. The op amp output Vtr is passed through SOV Checker and results in Vp/f. If Vp/f is zero, the circuit is faulty

otherwise it is fault-free. The Step signal generator and SOV checker are shown in figure 4 and figure 5 respectively.

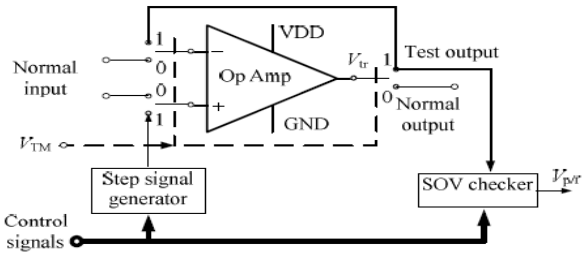

Fig-3: SOV BIST Architecture

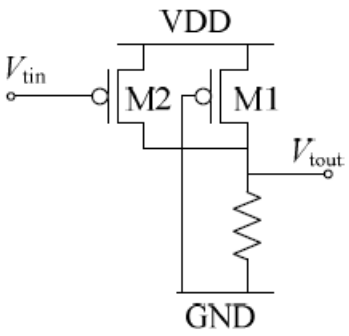

Fig-4: Step Signal Generator

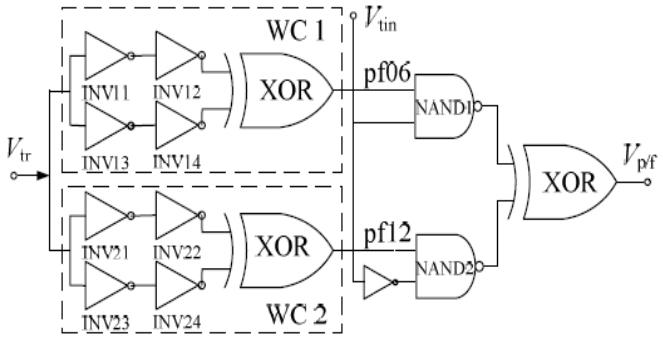

Fig-5: SOV Checker

The step signal generator consists of two PMOS transistors and a resistor. The W/L ratio of M1 is 3.4/0.4um and M2 is 2/0.4um.The resistor value is 1.615KΩ. When input is logic 1,M2 is off and only M1 conducts. So, the output is 0.607V.when the input is logic zero, both M1 and M2 conducts, so the output is 0.918V.Thus , a step signal is generated by the stimulus generator. The transistor parameters of SOV Checker are shown in Table 2.All others in the SOV Checker have the aspect ratio of 0.54/0.18.

TABLE-2: ELEMENT PARAMETERS OF SOV CHECKER

Elements	W/L (um)	Elements	W/L (um)
PMOS in INV11,INV12	0.6/0.4	PMOS in INV21,INV22	36/0.4
NMOS in INV11,INV12	4/0.4	NMOS in INV21,INV22	0.6/0.4
PMOS in INV13,INV14	0.6/0.4	PMOS in INV23,INV24	33/0.4
NMOS in INV13,INV14	2.4/0.4	NMOS in INV23,INV24	0.6/0.4

The circuit diagram of the Two-Stage Op Amp used in this test is shown in figure 6.The elemental parameters are shown in Table 3.

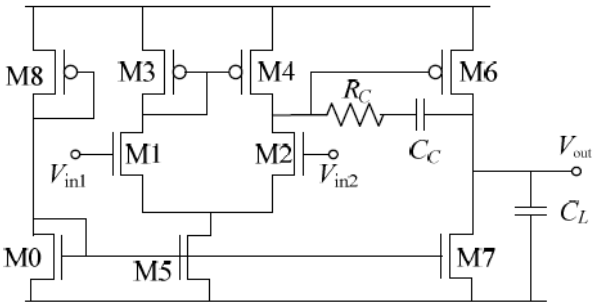

Fig-6: Circuit of Two-Stage Op Amp

TABLE-3: ELEMENT PARAMETERS OF TWO STAGE OP AMP

Elements	Size(Unit)	Elements	Size(Unit)
M0,M5	5.4/0.4 W/L (um)	M1,M2	5.4/0.4 W/L (um)
M3,M4	5.4/0.4 W/L (um)	M6	5.4/0.4 W/L (um)
M7	5.4/0.4 W/L (um)	M8	5.4/0.4 W/L (um)
Rc	18KΩ	Cc	0.8pF
CL	10pF	---	---

5. RESULTS

The Schematics of Two Stage Op Amp and CMOS Oscillator are shown in figure 7 and 8.

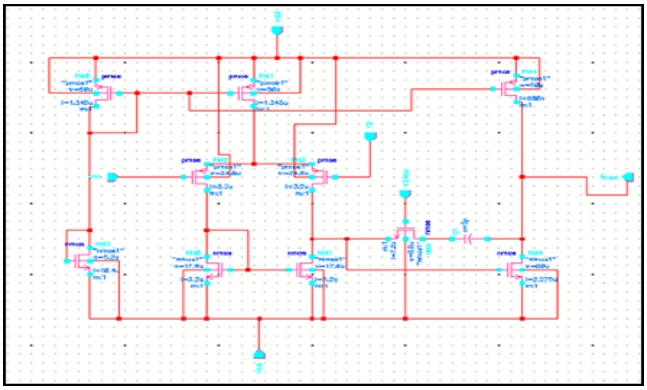

Fig-7: Schematic of Two Stage Op Amp

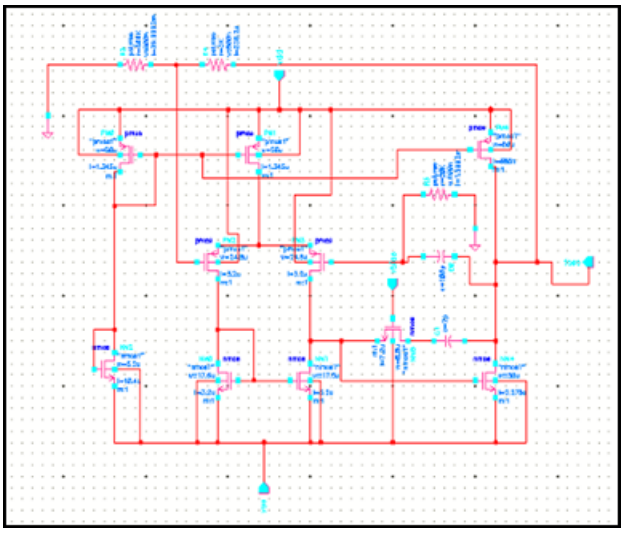

Fig-8: Schematic of CMOS Oscillator

CMOS Oscillator produces oscillations.By adjusting the feedback components sustained oscillations can be obtained.When faults are introduced, then, there will be deviation from natural oscillation frequency or there will not be any oscillations at all.Thus the faults can be detected in this method.Totally 57 faults were introduced and 53 faults could be detected.The faults includes both open and short(bridge)faults.So, the fault coverage was 92.98%.The Oscillations obtained by fault-free circuit and faulty circuit are shown in figure 9 and 10.

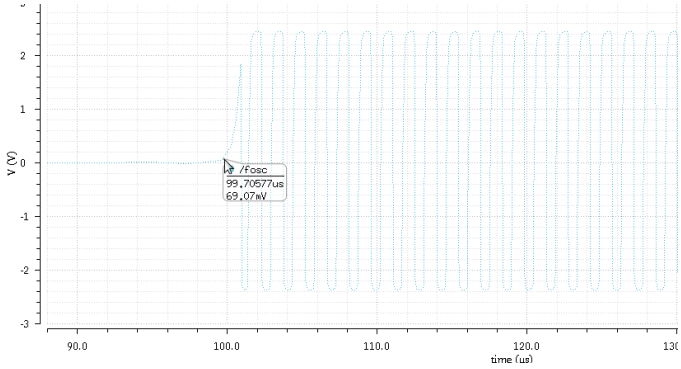

Fig-9: Transient Response of Fault-free circuit

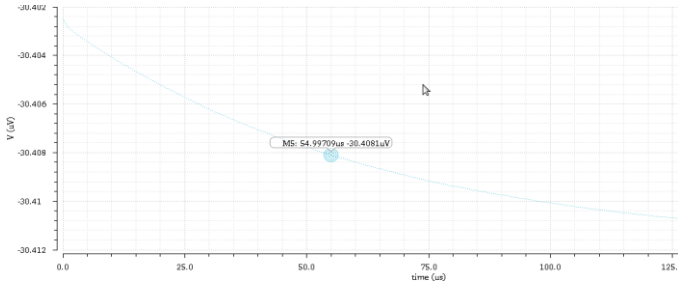

Fig-10: Transient Response of Faulty Circuit

The Schematics of Step signal generator, Op Amp and SOV Checker are shown in figure 11,12 and 13.

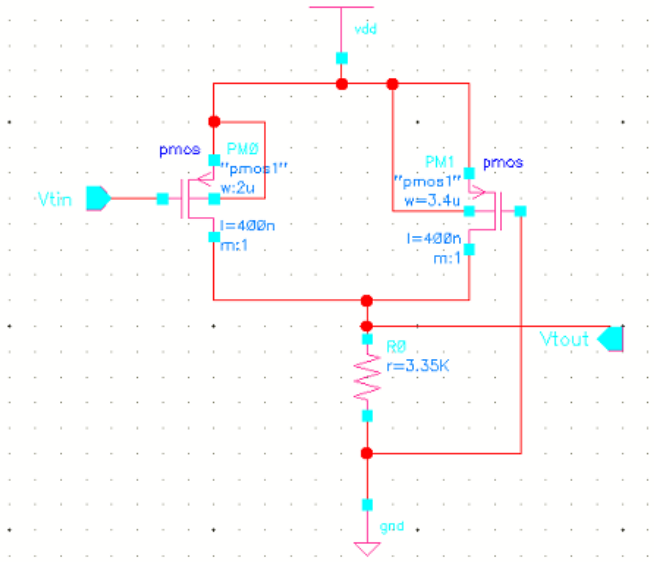

Fig-11: Schematic of Step Signal Generator

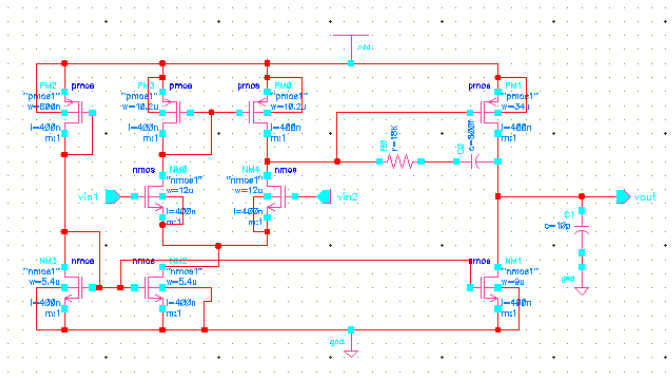

Fig-12: Schematic of Two Stage Op Amp

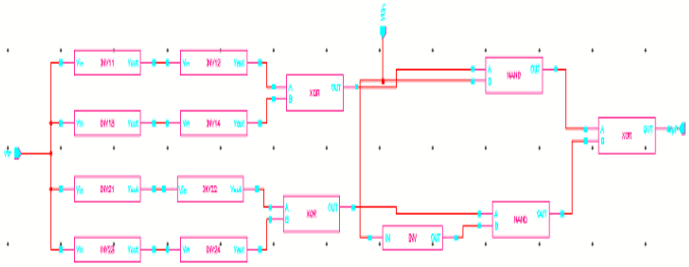

Fig-13: Schematic of SOV Checker

The signal generator output is given to the Op Amp .The Op Amp output is given to the SOV Checker.SOV Checker consists of two window comparators.WC1 outputs value when dc input is from 0.775V to 0.963V.WC2 outputs value when dc input is from 1.04V to 1.32V.So, at these voltages, the Vp/f is logic high for fault-free circuit and it is zero for faulty circuit. Since it is analog design, the voltage is in nano volts for faulty instead of zero. There were 54 faults introduced and 39 were detected. So, the fault coverage is 72.22%.The Vp/f waveform for fault-free and faulty circuit are shown in figure 14 and 15.

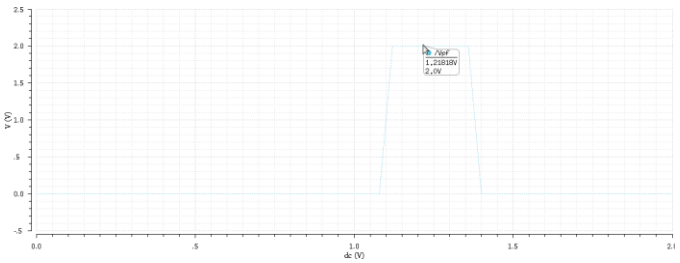

Fig-14: Waveform of Vp/f for a fault-free circuit

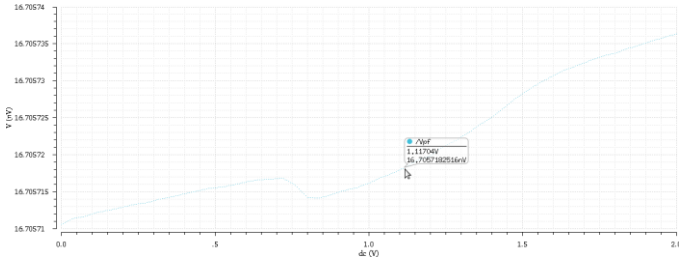

Fig-15: Waveform of Vp/f for a faulty circuit

Table 4 gives the comparison of both OTM and SOV Technique.

TABLE-4: COMPARISON OF OTM AND SOV CHECKING METHOD

METHOD	FAULTS INJECTED	FAULTS DETECTED	FAULT COVERAGE
OTM	57	53	92.98%
SOV METHOD	54	39	72.22%

6. CONCLUSION

This paper implements Oscillation based Testing Methodology and SOV based checking Methodology.OTM does not need any stimulus generator or response analyzer. But it's feedback capacitor results in area overhead and circuit complexity.SOV Method needs a step signal generator and SOV checker. This results in area overhead. The testing time also more in this. But in these two techniques, OTM has more fault coverage than SOV Method. The BIST Techniques has to be improved to prove lesser area, short testing time and more fault coverage.

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