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IMPLEMENTATION OF HALF SUBTRACTOR AND FULL SUBTRACTOR BASED ON CNTFET

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Abstract - *In digital signal processing (DSP), image processing and performing reckoning operations in microprocessors subtractor plays an important role. This paper advises the design of an energy efficient, high speed and low power half subtractor and full subtractor based on CNTFET. As far as it is known, this is the first attempt to design half subtractor and full subtractor using CNTFET. Results of the perfect design has been performed in 32nm technology and on comparison with a CMOS Technology based subtractor. Hspice mockups have been achieved on the subtractor designed using the modelled CNTFET.*

Key Words: **Carbon Nanotube (CNT), Carbon Nanotubes Field Effect Transistor (CNTFET) technology, CMOS Technology.**

1. INTRODUCTION

In VLSI technology, to any speed up the operation or reduce the power/vigor consumption hardware execution of many applications such as multimedia processing, digital communication can be possible. Arithmetic circuits are important part of Digital circuits. In the digital circuits, subtractor is one of the most critical components used in the processor of portable devices. Hence the power efficient, small delay design of Subtractor is necessary for design of small size portable devices. The recital estimation of 1- Bit half subtractor and full Subtractor is based on delay and power consumption. In the recent years, various approaches of CMOS 1-Bit half subtractor and full Subtractor design using various logic styles have been presented and unified into an integrated design policy which shows more delay and consumes more power.
Subtractor is a combinational circuit which represents the smallest unit for subtraction in digital systems. It is not only used for arithmetic calculation in many device processors but also used in other part of processor for calculating address. Stack pointer use subtraction operation in push-pop logical operation for storage of address. The simplest combinational circuit which performs the arithmetic subtraction of two binary digits is called half- Subtractor and full subtractor.

1.1 CNTFET

Carbon nanotube field effect transistor (CNTFET) are currently painstaking, one of the main building block for the spare of MOSFET based CMOS technology. The core of a CNTFET is carbon nanotube. CNTs are the echoing cylinders. Fig (1) shows the structure of graphene sheet and single walled carbon nanotube (SWCNT).

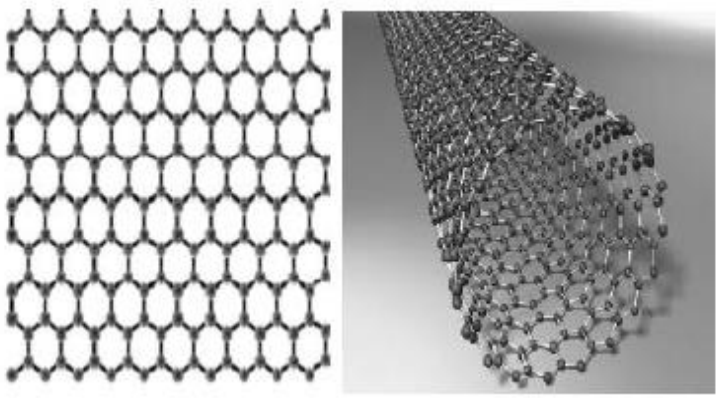

Fig.1: Structure of Graphene and SWCNT

Carbon nanotubes are formed, when a graphene sheet of a certain size that is swathed in a certain direction, it may be either sole walled or multi-walled. Two atoms in the graphene sheet are elected, one of which servers the role as origin. The sheet is rolled until the two atoms coincide. The vector grout from the first atom towards the other is called the chiral vector and its length is equal to the fringe of the nanotube. Liable on their chiral vector, carbon nanotubes with a small diameter are either semi-conducting or metallic in nature [6].

Carbon nanotube field effect transistors (CNTFETs) operate semi leading single-wall CNTs to assemble electronic devices. A single-wall carbon nanotube (or SWCNT) consists of one cylinder only, and the simple trade process of this

device makes it very gifted alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (*n, m*). The diameter of the CNT can be calculated based on the following equation [1] & [2].

$$D_{CNT} = \frac{\sqrt{3}}{\pi} a_0 \sqrt{n^2 + m^2 + nm} \qquad (1)$$

where a0 = 0.142 is the inter-atomic distance between each carbon atom and its neighbor. Like the MOSFET device, the CNTFET has also four terminals. The current-voltage (I-V) physiognomies of the CNTFET are like MOSFET's. The threshold voltage is defined as the voltage required to turn on transistor. The threshold voltage of the intrinsic CNT channel can be approached to the first order, as the half band gap is an inverse function of the diameter and the equation for threshold voltage is given below.

$$Vth \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}} \qquad (2)$$

where *a* = 2.49 Å is the carbon to carbon atom distance, Vπ = 3.033 eV is the carbon π-π bond energy in the tight bonding model, *e* is the unit electron charge, and *DCNT* is the CNT diameter. As *DCNT* of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels, is 0.293V, the device channel consists of a (19,0), zigzag CNT with a band gap of 0.53 eV and a diameter of 1.5 nm.

2. HALF SUBTRACTOR & FULL SUBTRACTOR

I. HALF-SUBTRACTOR CIRCUIT

Half-subtractor is used to subtract one binary digit from another to give DIFFERENCE output and a BORROW output. The truth table of a half-subtractor is shown in figure. The Boolean expressions for half-subtractor are, D=A'B+AB' & Bo=A'B. Here, the DIFFERENCE i.e. the D output is an EX-OR gate and the BORROW i.e. Bo is AND gate with complemented input A. Figure (2) shows the logic implementation of a half-subtractor. Comparing a half-subtractor with a half-adder the expressions for SUM and DIFFERENCE outputs are same. The expression for BORROW in the case of the half-subtractor is same with CARRY of the half-adder. However, the case of BORROW output the minuend is complemented and then ANDing is done. A half subtractor is a combinational logic circuit that subtracts one bit from another. This circuit has two inputs, the minuend and the subtrahend bits, and two outputs the difference and borrows bits. The truth table shown in Figure-(3) is constructed from the binary arithmetic operations. A practical use of half subtractor is for full subtractor in a digital system. Figure (2) shows the logic symbol of half subtractor.

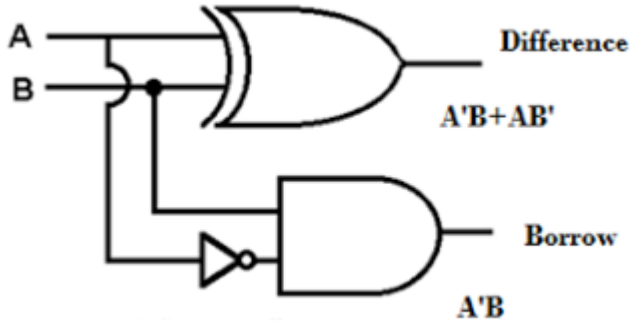

Fig -2: Half Subtractor

Inputs		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Fig -3: Truth Table of Half Subtractor

II. FULL SUBTRACTOR CIRCUIT

Full subtractor makes subtraction of two bits, one is minuend and other is subtrahend. In full subtractor '1' is lent by the previous adjacent lower minuend bit. Hence there are three bits are measured at the input of a full subtractor. There are two outputs, that are DIFFERENCE output D and BORROW output Bo. The BORROW output indicates 'that the minuend bit requires borrow '1' from the ensuing minuend bit. Figure (5) shows the truth table of a full subtractor. If we compare DIFFERENCE output D and BORROW output Bo with full adder 'it can be seen that the DIFFERENCE output D is the same as that for the SUM output. Further, the BORROW output Bo is like CARRY-OUT. In the case of a half-subtractor, an input is accompanied similar things are carried out in full subtractor. A full subtractor is a combinational circuit that performs a subtraction between two bits, considering borrow of the lower noteworthy stage. A full subtractor can also be implemented with two half-subtractors and one OR gate. The difference output from the second half-subtractor is the exclusive-OR of B_{in} and the output of the first half-subtractor, which is same as variance output of full subtractor. This circuit has three inputs and two outputs. The three inputs

are A, B and B_{in}, signify the minuend, subtrahend, and previous borrow, singly. The two outputs, D and B_{out} represent the difference and output borrow, respectively.

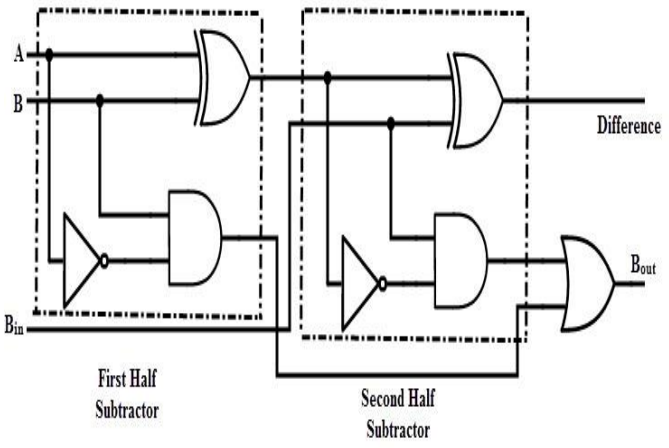

Fig -4: Full subtractor

The simplified logic equations from truth table are-

$$Difference = A'B'B_{in} + A'BB_{in}'+AB'B_{in}'+ABB_{in}$$
$$Borrow = A'B'B_{in}+ABB_{in}+A'B$$

Where A, B, B_{in} are the inputs. Outputs are denoted by difference and borrow (Bout) as shown in fig (4) of full subtractor.

Inputs			Outputs	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Fig -5: Truth Table of Full subtractor

3. LAYOUT SIMULATION

The layout is stick diagrammatic representation of CMOS Half subtractor and full subtractor showing NMOS, PMOS, P-diffusion, Metal Connect, N – diffusion Layers with A, B as the inputs and Difference, borrow as the outputs as shown in fig. (2) and fig. (4) respectively. These layouts help as a reference model to construct a complete half subtractor and full subtractor.

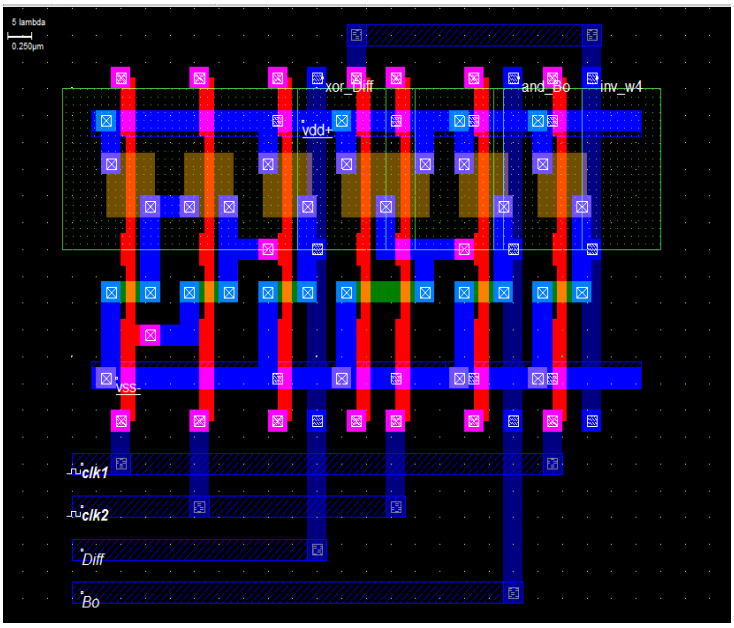

Fig -6: Layout of Half subtractor

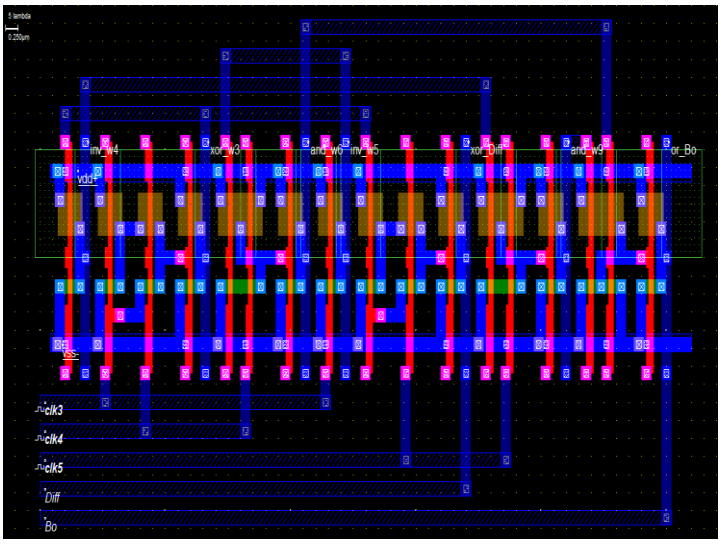

Fig -7: Layout of Full subtractor

A simple domino logic circuit consists of a pull-down network, a P-type pull up transistor, an N-type footer transistor a keeper transistor and an inverter. The clock signal is linked to the gates of p-type pull up and n-type footer transistors. When clock goes low, the dynamic node is pre-charged to VDD and the output goes low in this condition. When the clock signal goes high the circuit evaluate the logic function. The proposed Half Subtractor

circuit uses one 2-bit X-OR, one 2-bit AND & one inverter and for Full subtractor uses 2 half subtractor and one 2-bit OR gate circuits as shown in fig (2) and fig (4).

4. RESULTS

A binary Half-Subtractor subtracts two input bits and gives two output bits with one of them determining the difference (D) of the two input bits while the other giving the borrow bit (Bout). While, full subtractor subtracts two bits, '1' is borrowed by the previous adjacent lower minuend bit. Hence three bits are inputs and difference (D) and borrow (Bout) are outputs. The proposed Subtractor are compared based on the concert structures like Power, delay, max. Current. To achieve better performance, the circuits are designed using CNTFET technology at 32nm technology. The output waveforms outcome of proposed half subtractor and full subtractor circuit using 32nm CNTFET and CMOS technology, shown in Fig. (8), Fig. (9), Fig. (10), Fig. (11).

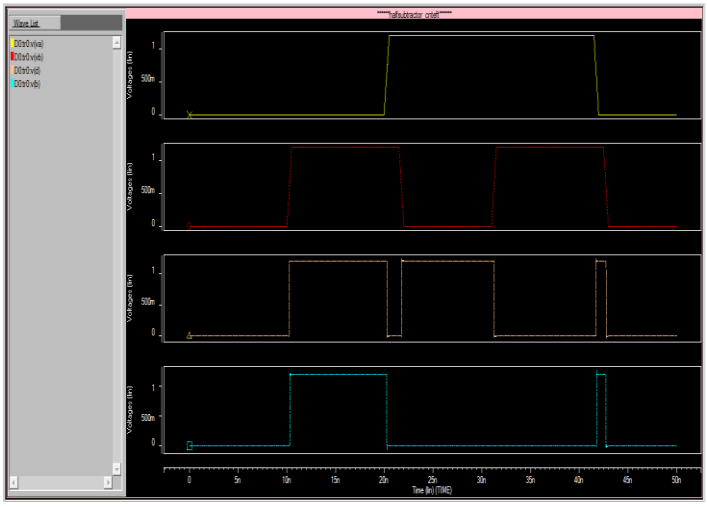

Fig -8: Half subtractor using CNTFET

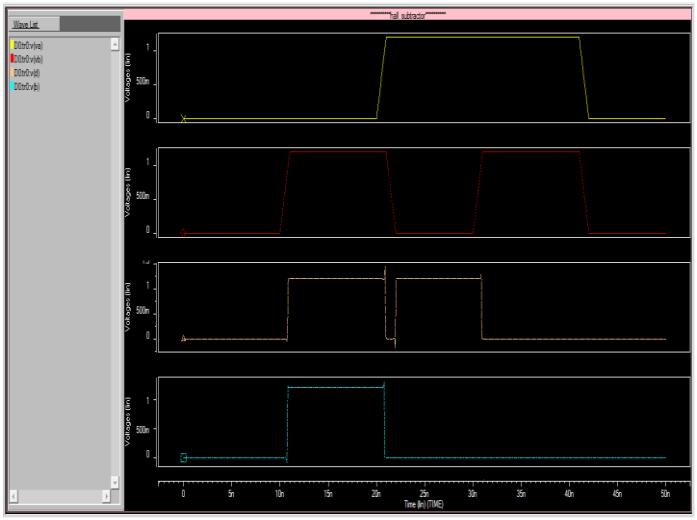

Fig -9: Half subtractor using CMOS

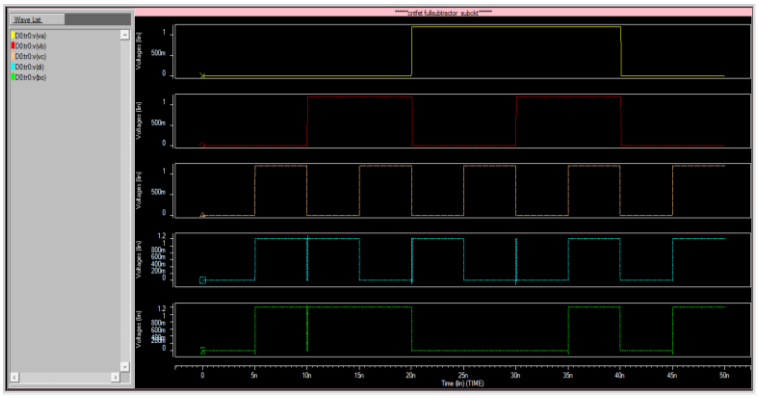

Fig -10: Full subtractor using CNTFET

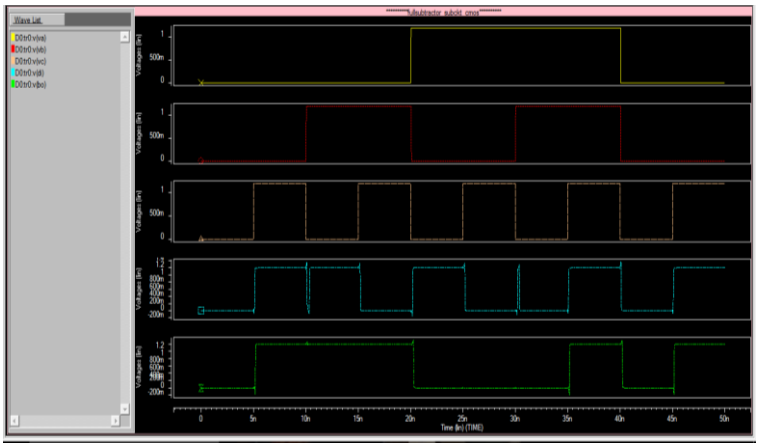

Fig -11: Full subtractor using CMOS

5.RESULTS WITH COMPARISION

PARAMETERS	Half subtractor		Full subtractor	
	CMOS (32nm)	CNTFET (32nm)	CMOS (32nm)	CNTFET (32nm)
Max. Current	5.3933uA	1.3068uA	21.587uA	4.4653uA
Power	8.3824nW	2.546nW	14.943nW	4.297nW
Delay	20.391n	11.015n	10.325n	4.9825n

6. CONCLUSIONS

In this paper, a half subtractor and full subtractor is proposed at 32nm using CNTFET technology and likened with CMOS technology. The performance of the half

subtractor and full subtractor has been evaluated and the proposed circuits are more superior when compared with CMOS technology and it is pragmatic that CNTFET based subtractor shows small delay, power and current. Using proposed design, Arithmetic Logic Unit and many more digital circuits can be designed and compared with low power applications.

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BIOGRAPHIES

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