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Design and Implementation of Low Power 16-bit Carry-lookahead Adder Using Adiabatic Logic

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Abstract*: This paper proposes a two-phase clocked adiabatic static CMOS logic (2PASCL) method for 16bit carry-lookahead adder. The 2PASCAL circuits working on the principles of adiabatic switching can be used for energy recovery. Adders are important components in applications such as digital signal processor (DSP) architectures and microprocessors. Apart from the basic addition, adders are also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. A schematic and layout of proposed circuit is implemented in Cadence Virtuoso 6.1.5 using 180nm technology. Further power dissipation comparison is made between 2PASCAL and standard CMOS, it shows a significant power saving.*

Key Words: 2PASCL adiabatic logic, Carry-Look Ahead Adder, Energy recovery, Power supply, Cadence Virtuoso.

1. INTRODUCTION

A demand for portable devices with low power consumption is requirement of today's electronics world. It is not possible for a customer to carry big batteries with them or charge the battery frequently. If device dissipates more power, internally it heats the system. To cool down the system it requires cooling mechanism, heat sinks and fans. But the device will become more bulky and expensive. For this reason VLSI designers have come up with new approaches to design a VLSI circuit, which consumes less power with increased battery life of a device. Adiabatic logic is one of them, where energy stored at the output node capacitance can be recovered back to the voltage supply. This technique is also referred to as "**REVERSIBLE LOGIC**". Static CMOS suffers from power dissipation when a transition occurs in the inputs and a direct path is formed from power supply to ground. Even there is power dissipation when capacitance is discharged through ground, and therefore there is waste of energy. Figure1 shows a charging and discharging path of load capacitance in CMOS logic.

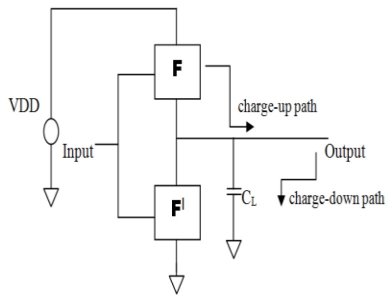


Fig -1: Conventional CMOS charging and discharging.

In CMOS circuits charges are fed from the power supply, steered through MOSFET devices, and then dumped into the ground terminal. To change a node's voltage with associated capacitance C_L, the circuit is as shown in Figure 2.
The energy is extracted from the V_{dd} terminal.

$$Q = C_L V_{DD}^2 \text{......... (1)}$$

Energy is stored in capacitance

$$E_{charge} = \frac{1}{2} C_L V_{DD}^2 \text{........ (2)}$$

Energy is dissipated in the channel resistance and wire resistance, the amount of dissipated energy depends on the voltage and the amount of charge which flows through, and is independent of the resistance.

$$E_{diss} = \frac{1}{2} C_L V_{DD}^2 \text{............ (3)}$$

Later, when this node is connected to the ground, the stored energy is again dissipated. In a cycle, charge is converted into heat [1].

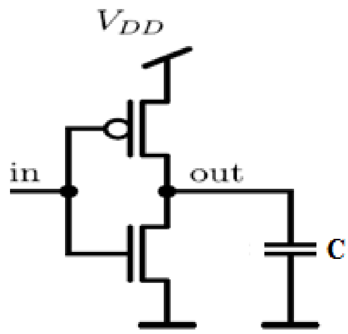


Fig -2: Schematic of a static CMOS inverter.

2. PRINCIPLE OF ADIABATIC SWITCHING

The word "***ADIABATIC***" comes from a Greek word that is used to describe thermodynamic process with no energy exchange with the environment and therefore, no energy loss in the form of dissipated heat [2].

In adiabatic logic a constant current source is used to charge and discharge load capacitance to reduce power dissipation in the circuits. To provide a constant current source AC voltage supply is used, a constant charging current corresponds to a linear voltage ramp whereas in CMOS logic a DC voltage supply is used.

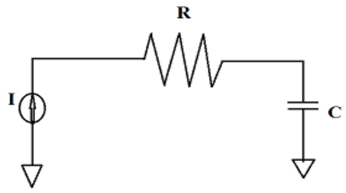


Fig-3: Adiabatic logic circuit.

The voltage across the switch is

$$V = IR \ldots\ldots\ldots\ldots (4)$$

Power in the switch,

$$P = I^2 R \ldots\ldots\ldots (5)$$

Energy during charging is

$$E_{Charge} = (I^2 R)T \ldots\ldots\ldots\ldots (6)$$

Where current is

$$I = C_L V_{DD}/T \ldots\ldots\ldots (7)$$

$$E_{Charge} = \left(R\, C_L \frac{V_{DD}}{T}\right)\left(C_L\, V_{DD}{}^2\right) \ldots\ldots\ldots (8)$$

Where-
C_L represents the Load capacitance.
R represents the on-resistance of PMOS.
V represents voltage at load capacitance.
T represents the charging time.

Figure 4 shows, implementation of adiabatic logic gate from static CMOS logic. Here a constant current source is used as power supply. The pull-up and pull-down networks can be connected as complementary transmission gate network. Power is applied to both pull-up and pull-down networks. Pull-up network will produce actual output and pull-down network will produce a complementary output (note: for complementary output the inputs applied to pull-down function should be complemented). Depending on inputs applied to the networks both the networks are used to charge-up or charge-down load capacitance [3].

Adiabatic logic family consist of many design techniques like efficient charge recovery logic (ECRL), 2N- 2N2P adiabatic logic, Positive feedback adiabatic logic (PFAL), Clocked adiabatic logic (CAL), Source coupled adiabatic logic (SCAL), Two phase adiabatic static clocked logic (2PASCL). In this paper INVERTER, NAND, NOR, XOR, CARRY-LOOKAHEAD ADDER (4 bit, 8 bit and 16 bit) circuits are presented. In this work we analyzed the performance of conventional CMOS adder circuits and adiabatic adder circuits in-terms of power consumption.

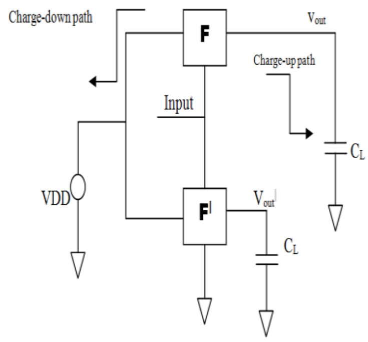


Fig-4: The topology of an adiabatic logic gate.

3. TWO PHASE ADIABATIC STATIC CLOCKED LOGIC (2PASCL)

In 2PASCAL logic, two diode circuits are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. 2PASCAL logic has two power supplies V_{fi} and V_{fibar}. As shown in figure 5, one diode (D_1) is connected between the output node and power clock (V_{fi}) and the other diode is placed adjacent to the NMOS logic circuit and connected to another power source (V_{fibar}). As name implies this logic operates in two phases EVALUATION and HOLD phase. In the EVALUATION phase V_{fi} will rise-up and V_{fibar} will fall-down. On the other hand, in the HOLD phase V_{fi} will fall- down and V_{fibar} will rise-up as shown in figure 6[4].

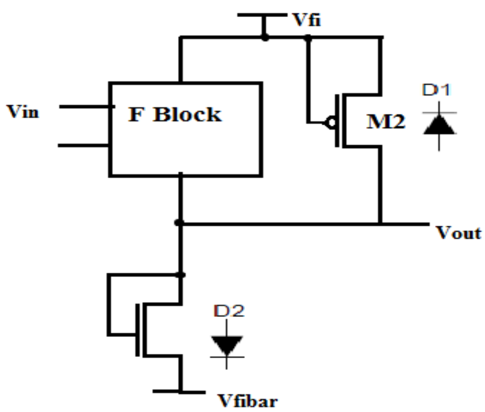


Fig-5: The basic structure of the adiabatic 2PASCAL logic.

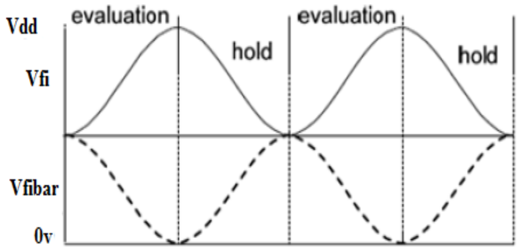


Fig-6: Power clocks in 2PASCAL.

3.1 Circuit Operation

Let us consider the inverter logic circuit as shown in Figure 7. In EVALUATION phase when input x is LOW, the transistor M_1 is turned ON and M_2, M_3 is turned OFF. C_L is charged through the PMOS transistor (M_1); hence, the output is in the HIGH state. There is no path between the output node and power supply V_{fibar}. In HOLD phase transistor M_3 is turns ON. The energy stored in load capacitance is discharged through transistor M_3 and power supply $V_{fibar.}$ When input x is HIGH the transistor M_2 is turned ON and M_1, M_3 is turned OFF. Since M1 is off C_L is not charged; hence, the output is in the low state [5].

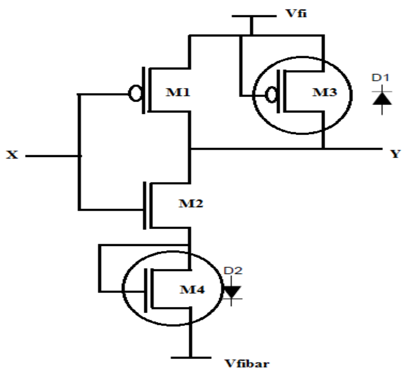


Fig-7: Schematic of the 2PASCAL inverter.

4. CARRY-LOOKAHEAD ADDER

To reduce propagation delay in ripple carry adder a carry-lookahead adder is implemented, it uses a special algorithm where inputs are decoded to generate carry information and form alternate and faster path to transfer carry bit. The corresponding Boolean expressions are given in the following section to construct a carry-lookahead adder. In the carry-lookahead circuit we need to generate two signals carry propagator (P) and carry generator (G) [6].

1) $P_i = A_i \oplus B_i$
2) $G_i = A_i \cdot B_i$

The output sum and carry can be expressed as

1) $S_i = P_i \oplus C_i$
2) $C_i+1 = G_i + (P_i \cdot C_i)$

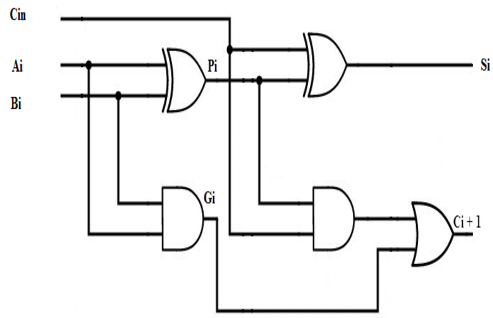


Fig-8: Carry propagate & generator.

5. DESIGN AND SIMULATION

A 2PASCAL adiabatic technique is designed using **CADENCE Virtuoso 6.1.5** for **schematic** with 180nm technology and **simulated** using **Spectre MMSIM131**.

5.1 Design and Simulation of an INVERTER using 2PASCAL Logic

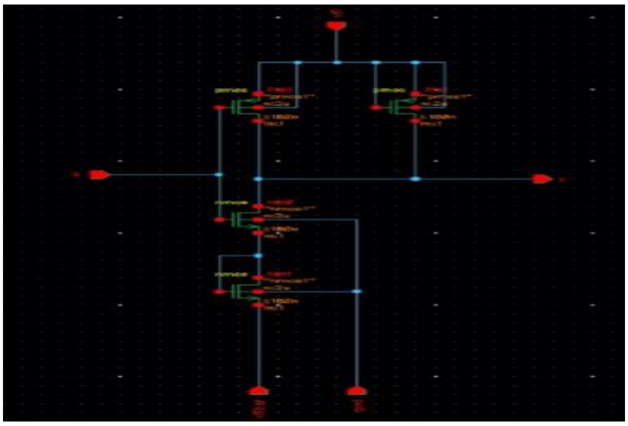


Fig-9: Schematic of 2PASCAL Inverter.

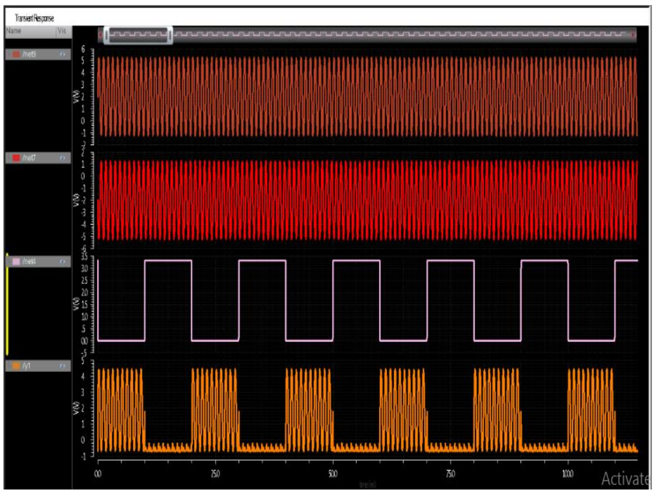


Fig-10: Simulation results of 2PASCAL Inverter.

5.2 Design and Simulation of Two Input NAND Gate using 2PASCAL Logic

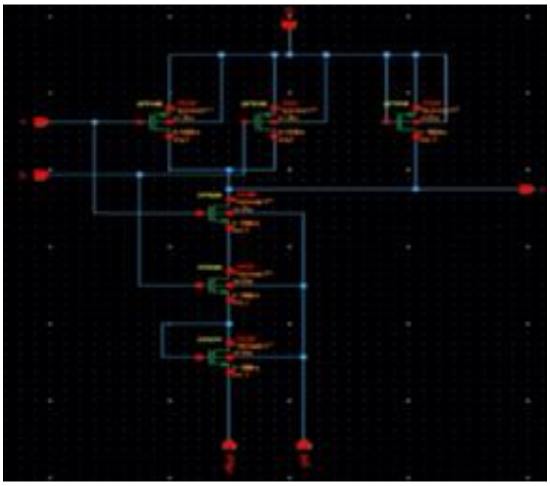


Fig-11: Schematic of Two-Input 2PASCAL NAND Gate.

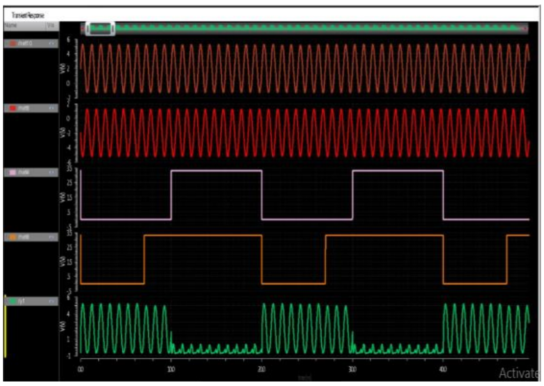


Fig-12: Simulation Results of Two-Input 2PASCAL NAND Gate.

5.3 Design and Simulation of Two Inputs NOR Gate using 2PASCAL Logic

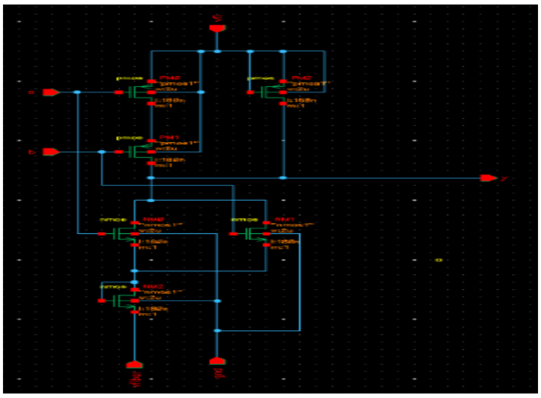


Fig-13: Schematic of Two-Input 2PASCAL NOR Gate.

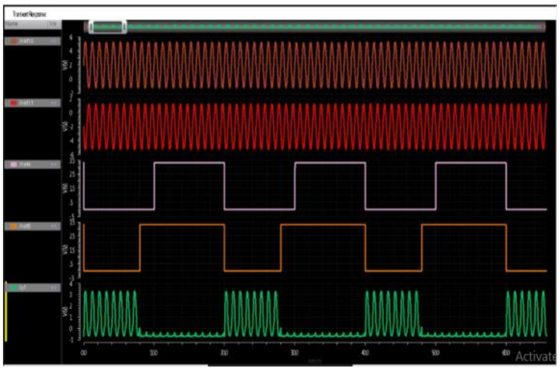


Fig-14: Simulation results of Two-Input 2PASCAL NOR Gate.

5.4 Design and Simulation of Two Input XOR Gate using 2PASCAL Logic

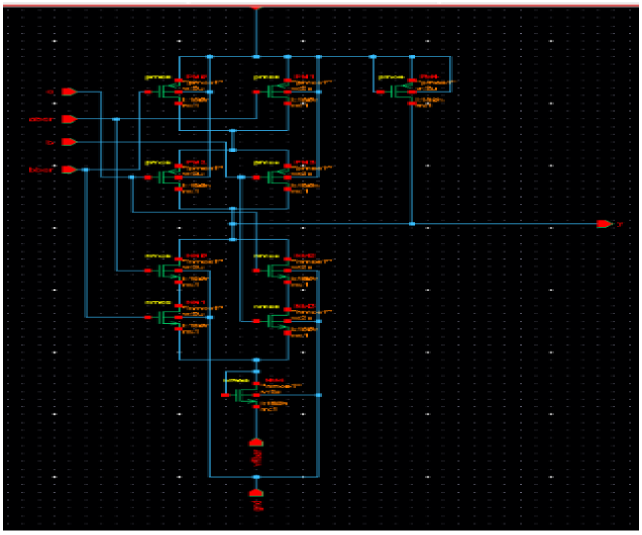


Fig-15: Schematic of Two-Input 2PASCAL XOR Gate.

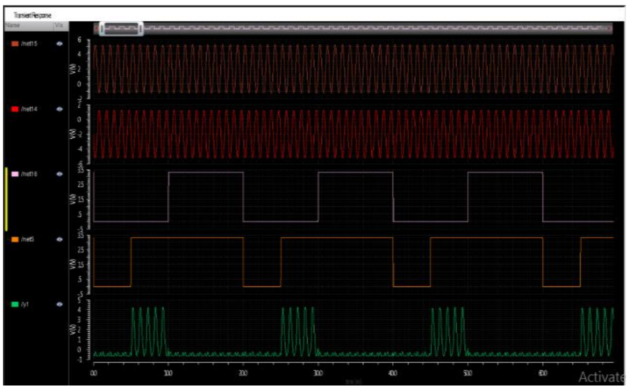


Fig-16: Simulation Results of Two-Input 2PASCAL XOR Gate

5.5 Design and Simulation of 4-BIT CARRY LOOK AHEAD ADDER using 2PASCAL Logic

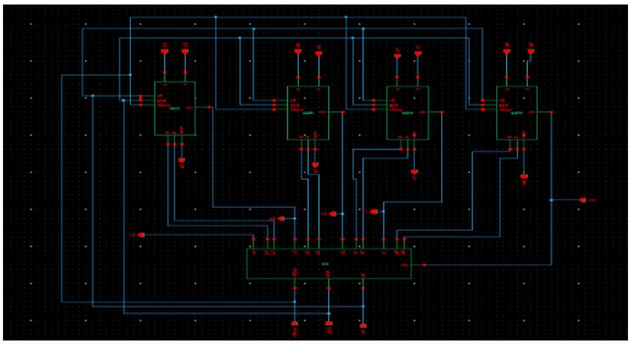


Fig-17: Schematic of 2PASCAL 4 bit carry-lookahead adder.

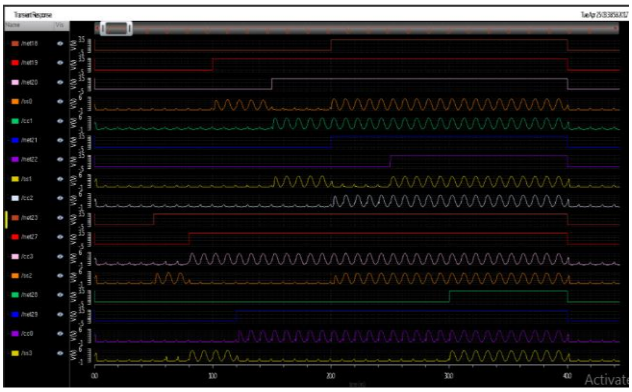


Fig-18: Simulation Results of 2PASCAL 4 bit carry-lookahead adder.

5.6 Design and Simulation of 8-BIT CARRY-LOOKAHEAD ADDER using 2PASCAL Logic

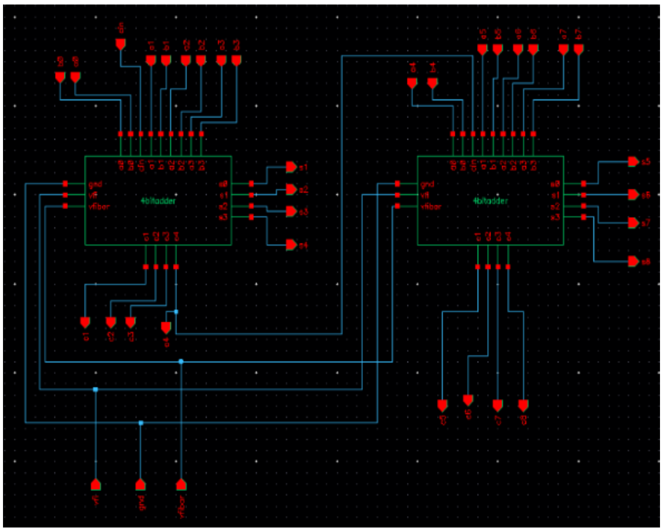


Fig-19: Schematic of 2PASCAL 8 bit carry-lookahead adder.

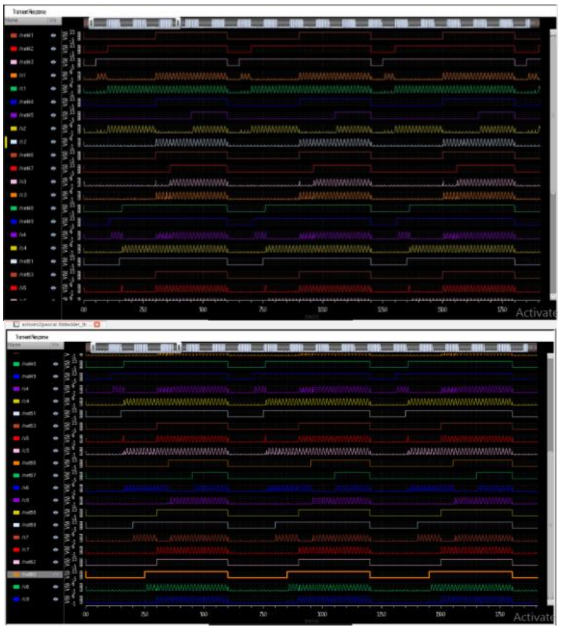


Fig-20: Simulation Results of 2PASCAL 8 bit carry-lookahead adder.

5.7 Design and Simulation of 16-BIT CARRY-LOOKAHEAD ADDER using 2PASCAL Logic

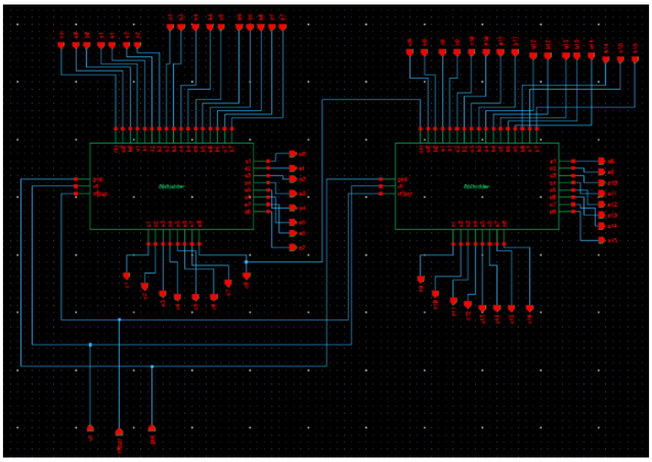
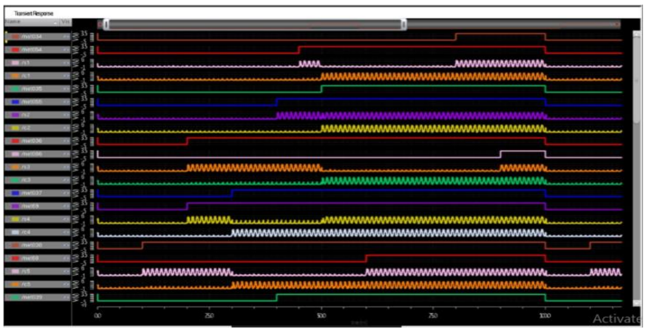


Fig-21: Schematic of 2PASCAL 16 bit carry-lookahead adder.



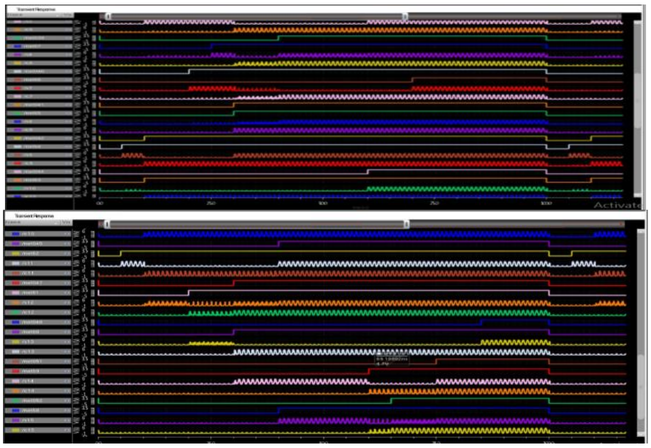


Fig-22: Simulation Results of 2PASCAL 16 bit carry-lookahead adder.

5.8 LAYOUT CELL DESIGN FOR AN ADIABATIC 2PASCAL 4-BIT CARRY-LOOKAHEAD ADDER

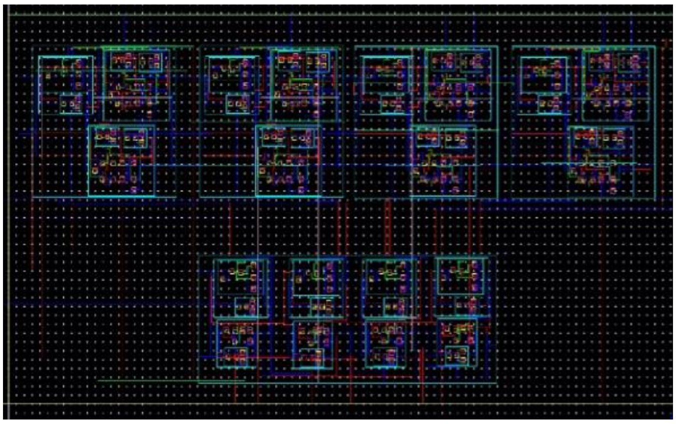


Fig-23: Layout of an adiabatic 2PASCAL 4-bit carry-lookahead adder.

5.9 LAYOUT CELL DESIGN FOR AN ADIABATIC 2PASCAL 8-BIT CARRY-LOOKAHEAD ADDER

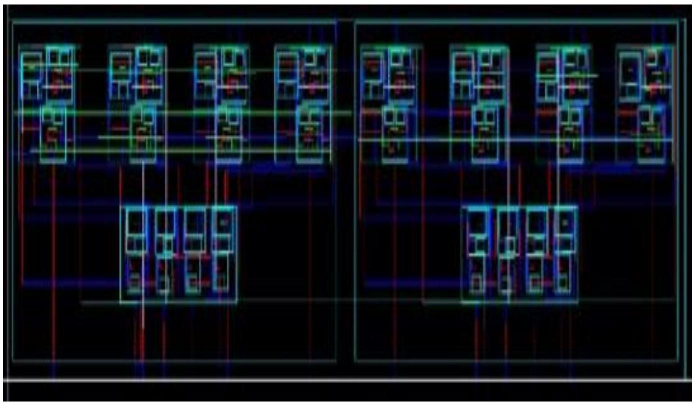


Fig-24: Layout of an adiabatic 2PASCAL 8-Bit Carry-Lookahead adder.

5.10 LAYOUT CELL DESIGN FOR AN ADIABATIC 2PASCAL 16-BIT CARRY-LOOKAHEAD ADDER

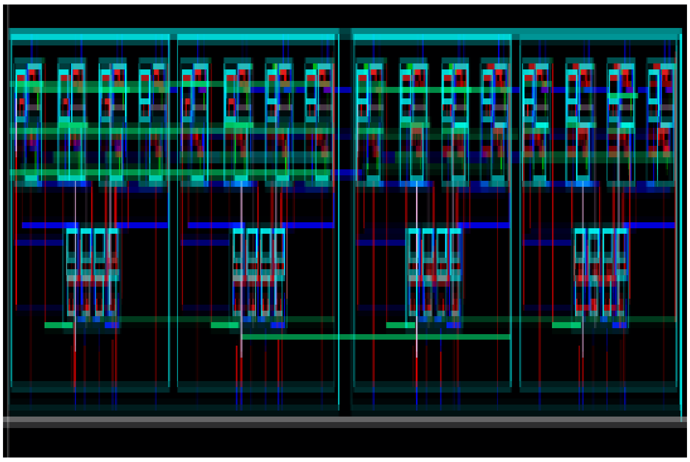


Fig-25: Layout of an adiabatic 2PASCAL 16-Bit Carry-Lookahead adder.

6. POWER DISSIPATION ANALYSIS

Power dissipation of a **2PASCAL** adiabatic technique is calculated using **Visualization and analysis CADENCE IC 6.1.6-64b.500.4.** Table 1 shows the average dynamic power dissipation comparison of inverter, Two-Input NAND gate, Two-Input NOR gate, Two-Input XOR gate, 4-Bit carry look ahead adder, 8-Bit carry look ahead adder, 16-Bit carry look ahead adder using static CMOS, 2PASCAL structures.

Table-1: Comparison between CMOS and 2PASCAL.

Design Logic	2PASCAL(uW)	CMOS(uW)
NOT	5.018	12.56
NAND	9.03	14.25
NOR	4.839	13.68
XOR	11.7	20.43
4-Bit ADDER	119.7	132.9
8-Bit ADDER	198.2	254.6
16-Bit ADDER	326.4	528.8

7. CONCLUSIONS

In this paper we have implemented two-phase clocked adiabatic CMOS logic (2PASCL) circuits and observed how it works in different phases of input power clock. The simulation results show that power consumption in the 2PASCAL NOT, NAND, NOR, XOR and 16 bit carry-lookahead adder circuits are considerably **less** than that in a static CMOS adder.

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