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DESIGN AND SIMULATION OF 1.2V TO 0.9V, 40mA LDO USING 90nm TSMC TECHNOLOGY

Naganagouda Linganagoudra[1], Sunil Kumar K H[2]

[1]PG Student (VLSI Design and Embedded Systems), Department of ECE, CMRIT, Karnataka, India
[2]Assistant Professor, Department of ECE, CMRIT, Karnataka, India

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Abstract - *Low Dropout Voltage Regulator (LDO) is a linear regulator which drives upon a very small differential voltage. The main components of the LDO are Error amplifier, Pass device and Voltage divider network. Two stage Operational amplifier is a Error amplifier which enhances the gain of the proposed LDO. NMOS pass device require more VDD compared to gate input voltage to overcome this charge pump circuitry is needed which results in the increase of noise. So PMOS pass device is used to overcome the disadvantage of NMOS pass device. Proposed LDO consists of input voltage is 1.2V, output voltage of 900mV and drop voltage is 300mV.The gain of LDO is obtained to be 68.18dB under no load condition and 58.39 under full load condition. The proposed LDO system is designed in the standard CMOS 90nm technology with Cadence virtuoso tool is used to implement this circuit.*

Key Words: **LDO, OPAMP, OTA, V_{ref}, V_{in}, V_{out}**

1. INTRODUCTION TO LDO

Power supply is one of the most important parameter for any integrated circuits. Power supply is responsible for the powering of the circuit. In any integrated circuits there are devices or components which may require different supply voltages for their proper operations. This done by branching the main power supply by the process called voltage level shifting. Depending upon the functionality, the power supply can be classified as unregulated power supply and regulated power supply. In regulated power it will provides constant output voltage irrespective of the load conditions and in unregulated power supply the output voltage will vary depending upon the load conditions. In most of the circuits it necessary to get constant voltage is which is well provided by Low Dropout Regulator (LDO).

The operational amplifier with folded cascode itself ought to give lower power dissipation and also its bias current streams required to be reserved as low as conceivable. It is obvious that a speed/dissemination exchange off emerges, and the fundamental impediment is showed regarding slew-rate of the error amplifier [1].

LDO's dropout voltage is limited to ensure superior power supply rejection at improved productivity. They are using dropout voltage of 300mV.The plan technique for acquiring the low quiescent current at correct precision in DC response present and quick transient output to fit in with the other circuit [1].

LDO voltage controllers result in a little voltage drops over the power device transistor and give a very much managed lower noise voltage. These devices are especially appropriate for convenient portable device applications, which require lesser noise. In convenient devices, a vital outline thought is diminishing quiescent current which result in expanded life expectancy of the battery.

2. LDO DEFINITION

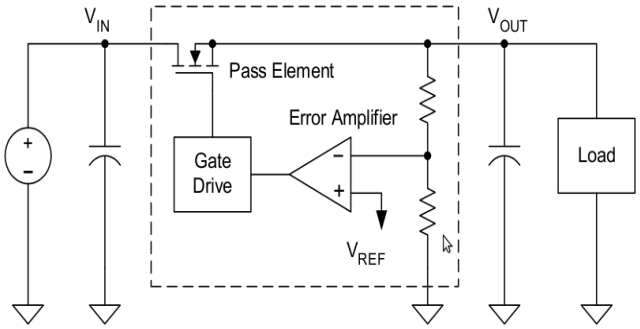
A series arrangement low-drop-out controller is a circuit that gives a very much determined and stable linear dc voltage for which output to input voltage distinction is low. The drop-out voltage is characterized as the estimation of differential voltage of input to output, where the control loop quits regulating.

The term series arrangement originates from the way that a power transistor is associated in arrangement of the input terminals to the output terminals of the controller. The function of the circuit depends on giving back an increased error signal for the control of the output current stream of the power transistor forcing the output load.

3. LDO BLOCK DAIGRAM

LDO block diagram is shown in the figure 1.The primary pieces of the regular LDO topology are the error amplifier, the pass transistor and the straight input arrange. To work, the LDO additionally needs a voltage reference. This reference is set up by an electric circuit known as Band Gap. The contrast amongst LDOs and Band Gaps, since both give a consistent voltage, is that a LDO must have the capacity to give current and voltage to any uncertain number of load steps

Fig -1: LDO Block Diagram [5]



4. LDO DESIGN

4.1 Design of Voltage Divider

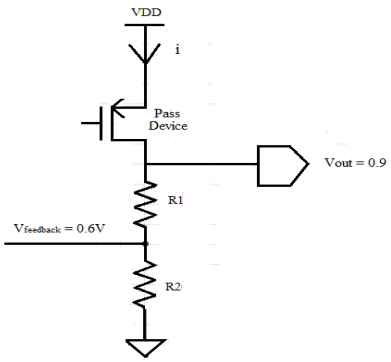


Fig -2: Voltage divider

Let's Assume $V_{feedback}$ =0.6V
Therefore, R_1=0.5R_2
Let choose R_1=1KΩ, therefore R_2=2KΩ

4.2 Design of Two stage Operational Amplifier

By considering DC gain of 60dB,Gain bandwidth of 30MHz,Phase margin of 60^0 and V_{DD} of 1.2V designed circuit for two stage operational amplifier with design specifications is shown in the figure 3 [7].

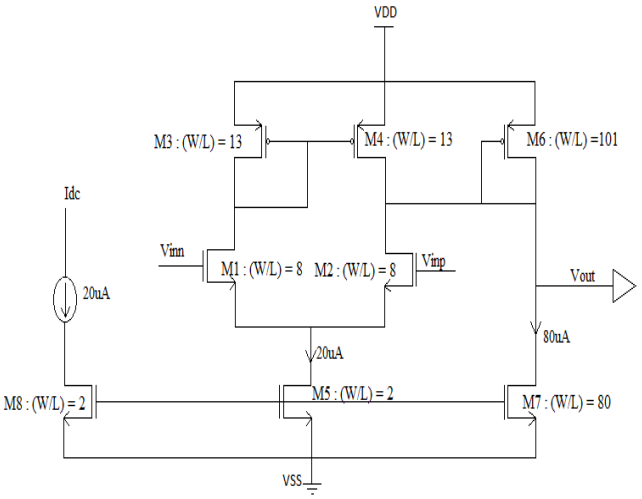


Fig - 3: Two stage OPAMP with Design Specifications

4.3 Design of Pass Device

For the design of pass device the circuit setup is shown in the figure 4. Supply voltage is 1.2V, output voltage across the drain is 900mV. Gate voltage is of 400mV which is the minimum voltage, that is required to enhance withdrawing current of 40mA. Width and Length of pass device are assumed to be 500n and 100n respectively now sweeping the finger of pass device to get 40mA current through it.

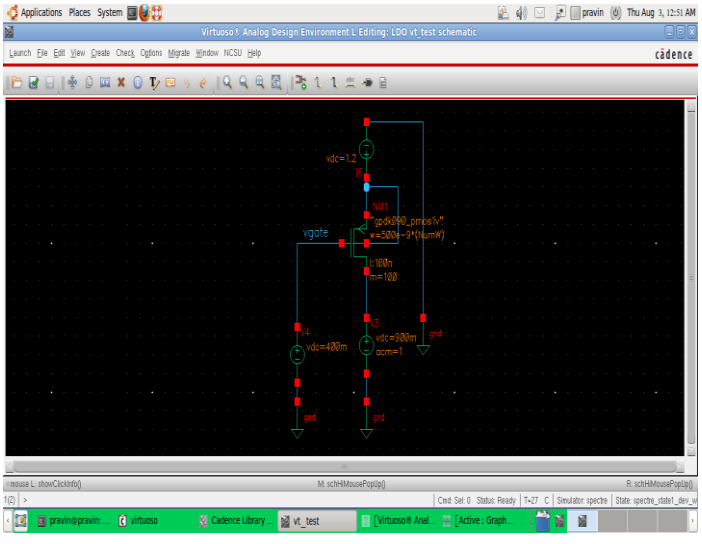


Fig -4: Set for Designing of Pass Device

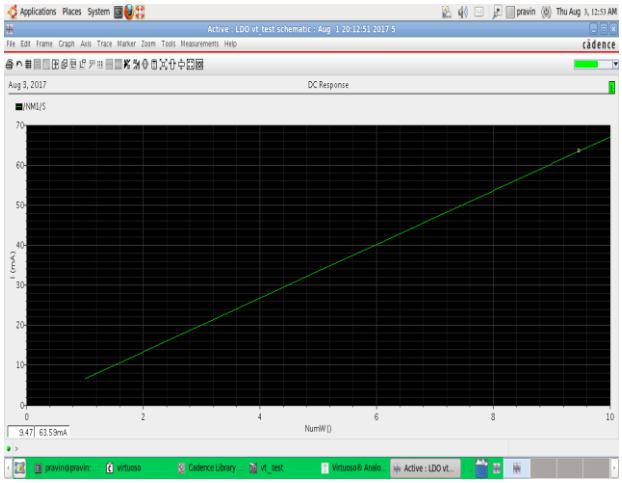


Fig -5: Current v/s Fingers of device

Figure 5 shows the graph of Current v/s Fingers of device. At fingers of 6 the current through the pass device is 40mA.so for the designing of LDO, Pass device with width and length of 500n and 100n with fingers of 6.

5. LDO RESLUTS

The simulation results are shown as in following figures

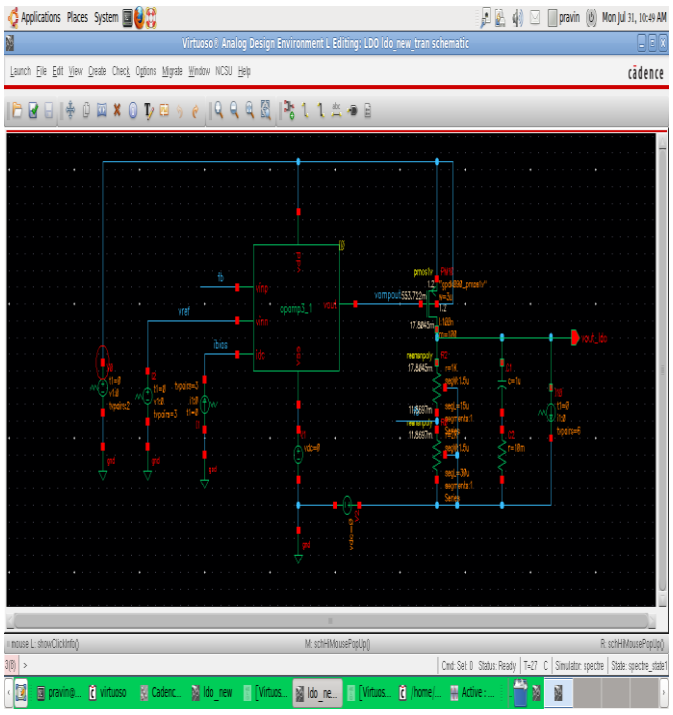


Fig -6 LDO DC Simulation Setup

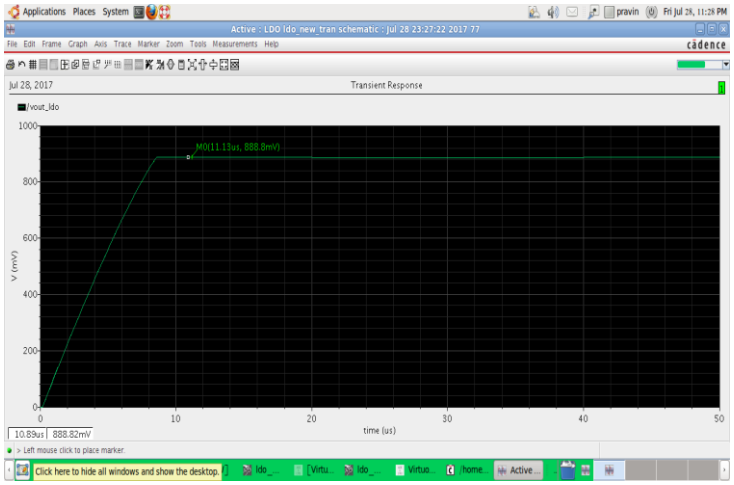


Fig -7: LDO Output

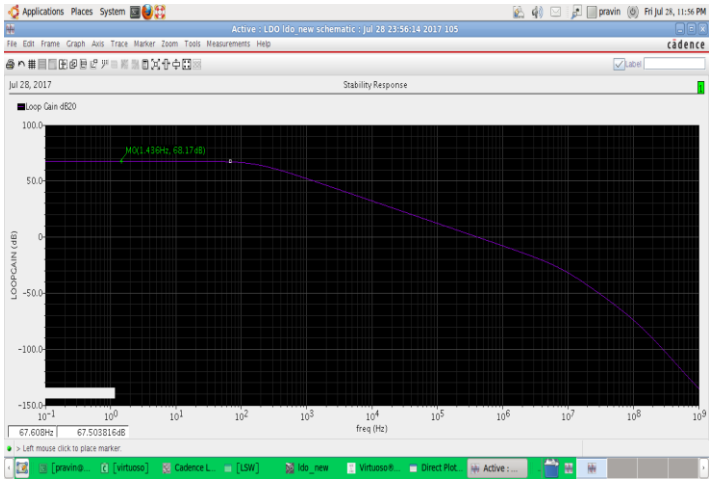


Fig -8: LDO gain

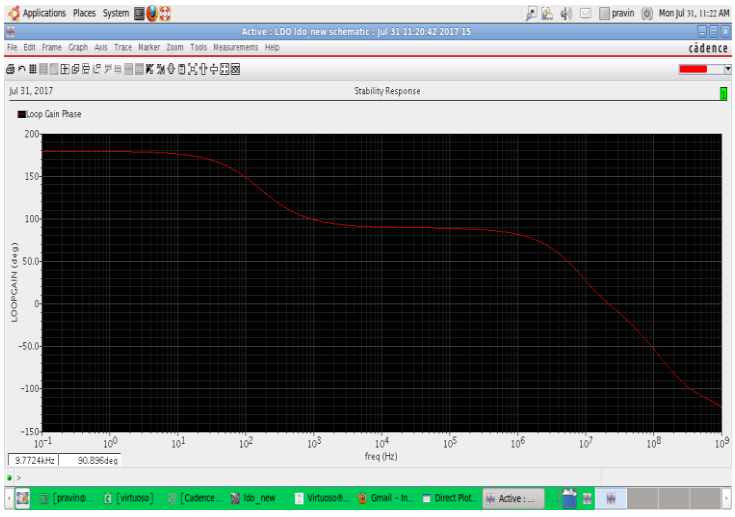


Fig -9: LDO Stability response

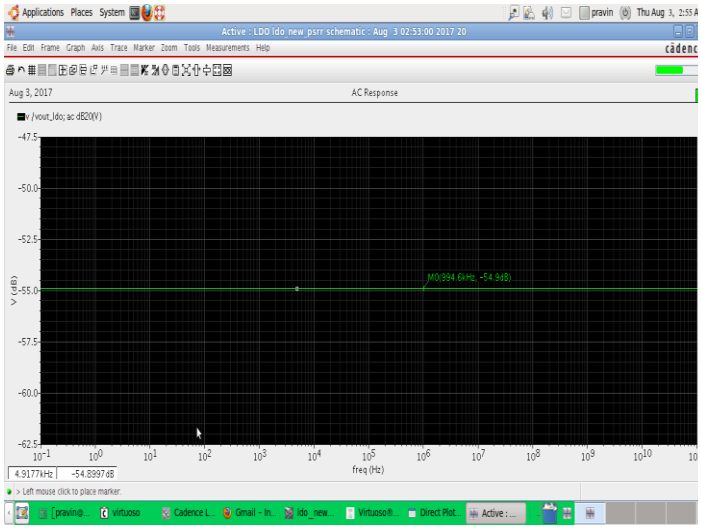


Fig -10: LDO's PSSR

Table 1 LDO's Specification

SI NO	Parameters		Condition	Specifications	Designed	Unit
1	1.Input voltage			1.2	1.2	V
2	2.Output voltage			900	888	mV
3	3.Load current			40	40.28	mA
4	4.Dropout voltage			300	312	mV
5	5.Output capacitance			1	1	uF
6	Gain	GM @ FL		60	58.39	dB
		GM@ NL		65	68.17	dB
		PM @ NL		90	86.98	Deg
		PM @ FL		55	45.43	Deg
7	PSSR	NL		-60@1Meg	-54.89	dB
		FL		-50@1Meg	-50.42	dB
8	Line Regulation	FL	line_reg_tran_1p2to1.7	0.1	0.8737	%
			line_reg_tran_1p7to1p2	0.1	0.07585	%
			line_reg_dc	0.1	0.095	%
		NL	line_reg_tran_1p2to1.7	0.1	0.063	%
			line_reg_tran_1p7to1p2	0.1	0.063	%
			line_reg_dc	0.1	0.063	%
9	Load Regulation		load_reg_tran_NtoF		0.166	%
			load_reg_tran_FtoN		0.136	%
			load_dc_tran_NtoF		0.012	%
10	Quiescent current			580	569	uA
11	Efficiency				97.29	%

6. CONCLUSION AND FUTURE SCOPE

The circuit is designed in the standard 90nm CMOS technology, with supply voltage of 1.2V and output voltage 900mV and the reference voltage is taken to be 600mV.Gain of the LDO system is obtained to be 68.18dB under no load condition, PSSR of -56dB at no load. PSRR is -54.89 at no load and -50.42 at full load condition. Line regulation obtained to be 0.063% at no load.

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