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Low Power High Speed 24 Bit Floating Point Vedic Multiplier using Cadence

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Abstract - *There is always an ever growing demand for high speed processing and low power design. It is known that multiplier unit forms an integral part of processor design. It performs core operations in many complex systems. Digital Signal Processing applications essentially require the multiplication of binary floating point numbers. For IEEE754 floating point multiplier design, Vedic Multiplication method is used. The ease of multiplication of Mantissa part is done by Urdhva Tiryakbhyam method. By using this method the number of adders as well as the delay at each stage has been reduced when compared with existing designs of conventional multipliers. Hence, the proposed multiplier shows substantial improvement in the floating point computation. This paper deals with the design of 24 bit floating point multiplier using Vedic mathematics and compares the result with conventional multiplier. Simulation of the design and Verilog coding is carried out using Xilinx ISE 12.1 software and Synthesis is performed using CADENCE Genus tool.*

Key Words: **Floating point multiplication, Urdhva-Tiryakbhyam, Vedic Mathematics…**

1. INTRODUCTION

Multiplier is an essential functional block of a microprocessor because multiplication is needed to be performed repeatedly in almost all scientific calculations. The fast and low power multipliers are required in small size wireless sensor networks and many other DSP (Digital Signal Processing) applications. They are also used in many algorithms such as FFT (Fast Fourier transform), DFT (Discrete Fourier Transform). There are two basic multiplication methods namely Booth multiplication algorithm and Array multiplication algorithm used for the design of multipliers. The schemes for efficient addition of partial products are Wallace tree, Dadda tree. The speed of multiplication (as well as power dissipation) is dominantly controlled by the propagation delay of the full adders and half adders used for the addition of partial products. Multipliers have large area, long latency and consume considerable power.

Processing applications is vastly reduced when signals are represented in the frequency domain. Fourier Transform analysis transforms a signal from its original domain to a representation in frequency domain and vice versa. Fast Fourier Transform [FFT] algorithm efficiently computes the DFT by factorizing the DFT matrix into a product of zero factors, and thereby reducing the computational complexity to 0[nlogn]. Fast Fourier transforms are globally used for various application fields in engineering, communication, and mathematics.

Nowadays, every process should be rapid and efficient. Fast Fourier transform is an effective algorithm to calculate the 'n' point DFT. Even though this algorithm has large range of applications in communication, signal and image processing, its Implementation needs great number of complex multiplication steps. So for our convenience and make the whole method simple and delay free, we need an efficient multiplier. To overcome this problem Urdhva Tiryakbhyam sutra (UT Sutra) is considered as an efficient method of multiplication [1].

The most widely used standard for Binary floating point computation is the Binary Floating Point IEEE754 Standard. Floating-point fixes a number of representation problems. Fixed point is restricted to a fixed limit which restricts it from representing very large or small numbers. Also when two large numbers are divided, a fixed point is exposed to loss of precision. Vedic mathematics mentioned on ancestral Indian Vedas gives a different multiplication algorithm to carry out fast multiplication. The Sutras Urdhava-Tiryakbhyam and Nikilam Sutras give easiest way of mental calculation when performing multiplication. Among these 2 sutras, Urdhva-Tiryakbhyam employs parallel multiplication and exhibits high degree of parallelism compared to other parallel multipliers.

2. ARCHITECTURE OF THE SYSTEM

2.1 Vedic Mathematics

Vedic mathematics is the name given to the old system of mathematics which was find out from the "Vedas". Because of the easiness of Vedic multiplication over conventional method, it can be easily adopted to practical situations. Swami Bharati Krishna Tirthaji Maharaj (1884-1960), re-introduced the concept of ancient system of Vedic mathematics [1]. The word 'Vedic' is derived from the word 'Veda' which means the storing house of all knowledge. The Sutrams Urdhava- Tiryakbhyam and Nikilam Sutrams give easiest way of mental calculation when performing multiplication. Vedic Mathematics is a

domain which gives various effective algorithms which can be applicable to various branches of Engineering such as digital signal processing and computing. The number of logic levels and logic delay is being reduced using the Urdhva- Tiryakbhyam sutra. Vedic mathematics is a mental calculation method that provides worldwide acceptance because of its easiness and advantages.

2.2 Urdhva Tiryakbhyam Sutra

The word **"Urdhva-Tiryakbhyam"** means "Vertically-crosswise" in Sanskrit. This multiplication method can be applied to all cases of algorithm for N bit numbers. Urdhva-Tiryakbhyam [UT Sutra] employs parallel multiplication and exhibits high degree of parallelism compared to other parallel multipliers. In conventional parallel multiplication method partial products get summed up after the generation of all partial products. In the case of Urdhva- Tiryakbhyam, multiplication vertically and crosswise means summation will takes place just after partial products for a column gets generated. This high degree parallelism gives better speed compared to other parallel multiplication.

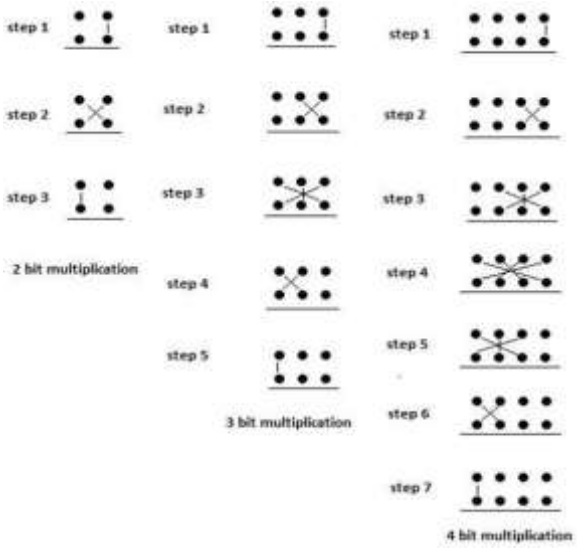

Fig -1: Line Diagram of UT sutra

Implementation of fast vedic multiplier will improve the performance of the current processors. Figure 1 shows the line diagram of UT sutra.

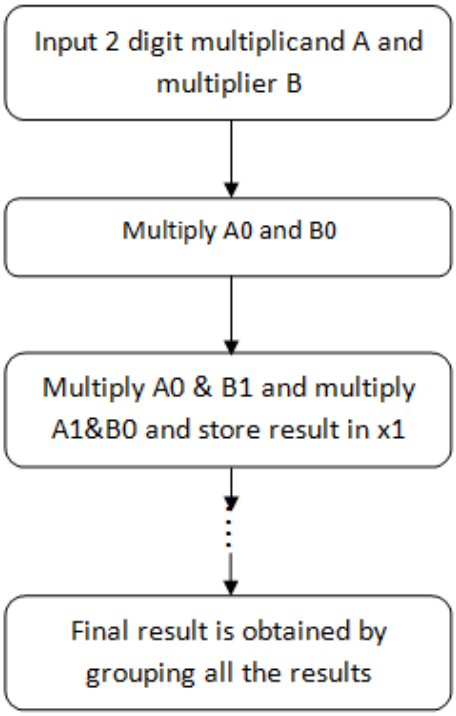

Fig -2: Vedic Multiplier Flow Chart

This Sutra shows how to multiply a large bit [N x N, of N bits] by breaking it into smaller numbers of size (N/ 2 = n, say) and these smaller numbers can again be broken into smaller numbers (n/2 each) till we reach multiplicand size of (2 x2) Thus, the entire multiplication process is simplified and is shown in figure 2.

2.3 Floating Point Multiplication

For DSP applications, IEEE 754 floating point standard is widely used today. The IEEE [Institute of Electrical and Electronics Engineers] defines a Standard for floating-point representation and arithmetic. This IEEE754 standard is the widely accepted representation for floating numbers even though there are many other representations. Consider a floating point number - $5.94 * 10^3$. The '-'symbol indicates the sign component of the number, the '594' indicates the significant digits of the number and at last the '3' indicates the scalar factor component of the number. The significant digits are termed as the *mantissa* of the number and scalar factor is called as *exponent* of the number

The general representation format is of the following and is shown in figure 3:

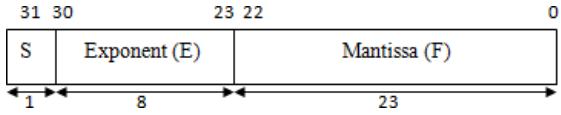

Fig -3: Single Precision IEEE 754 Floating Point Number Format

Where, S - Sign Bit, M – Mantissa Bits, E – Exponent

3. DESIGN STEPS OF SINGLE PRECISION FLOATING POINT MULTIPLIER

In this paper a Single precision floating point multiplier which can handle over flow, under flow and rounding of the result are designed. Figure 4 shows the multiplier structure that includes the addition of exponents, multiplication of mantissa, and sign calculation

3.1 Floating Point Multiplication Algorithm

Multiplication of two floating point binary digits represented in IEEE 754 format is interpreted as

V = (-1) ^Sign * 2^ (exponent - bias) * 1.fraction

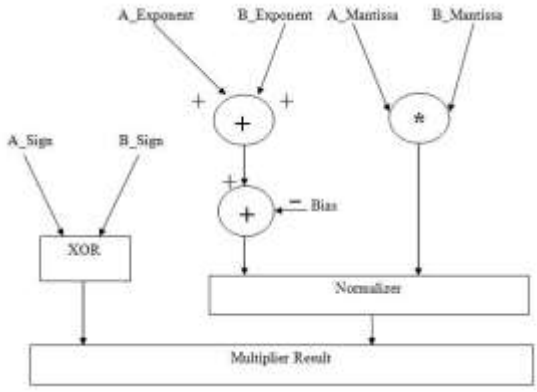

Fig -4: Floating point multiplier diagram

The steps for multiplying two floating point number is given below:

1. Multiply 2 significant bits; i.e. (1.M1*1.M2).
2. Place a decimal point in the result.
3. Add the exponent bits; i.e. (E1 + E2 – *Bias*).
4. For obtain the sign bits, do XOR of 2 bits; i.e. s1 xor s2.
5. Do Normalization of the result; i.e. obtaining 1 at the MSB of the result.
6. Truncating the results to fit in the available bits.
7. Checking the underflow and overflow cases.

4. PROPOSED VEDIC MULTIPLIER

The proposed design uses Vedic mathematics based on Urdhva Tiryakbhyam sutra for the multiplication of the mantissa part in IEEE 754 single precision floating point multiplication. In this proposed multiplier the base block used as first stage implementation is 3*3 block which is shown in figure 5. Here we need 24 bit Vedic multiplier for the multiplication of mantissa part.

The 3*3 block consists of two half adders, one full adder and three 2 bit adders as shown in figure 5. From this 3*3 block, 6*6 multiplier block is designed. From this 6*6 multiplier block, 12* 12 multiplier block is designed and similarly from this 12*12 multiplier block, 24*24 multiplier block is designed and implemented. These blocks require Vedic multipliers and ripple carry adders for getting the final output.

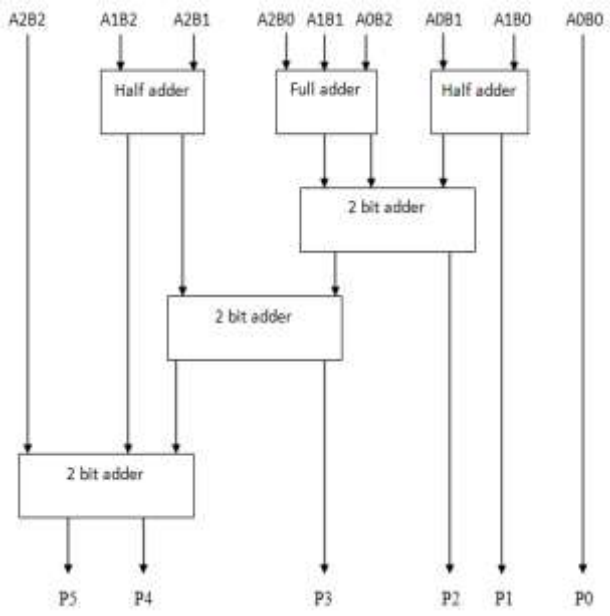

Fig -5: Architecture of 3*3 Block using UT sutra

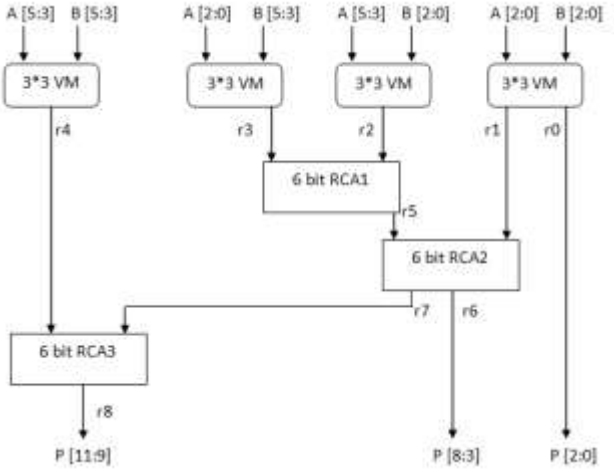

Fig -6: Architecture of 6*6 Block using UT sutra

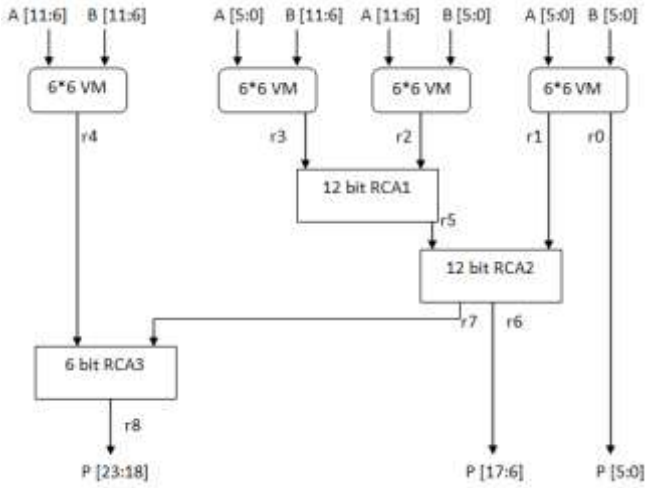

Fig -7: Architecture of 12*12 Block using UT sutra

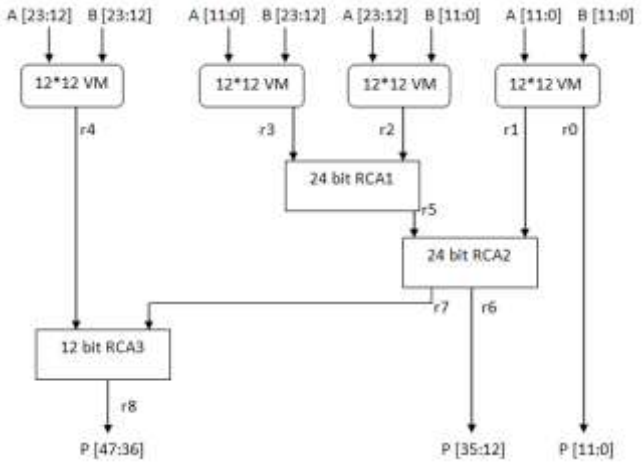

Fig -8: Proposed 24*24 Bit Vedic Multiplier

5. RESULTS

The design of IEEE 754 standard floating point Vedic multiplier using Urdhva-Tiryakbhyam method is performed and Synthesis of the design is performed using Cadence Genus tool. The synthesis results show that the parameters like Power, Area and CPU Timing is much less when compared to synthesis performed using Xilinx tool.

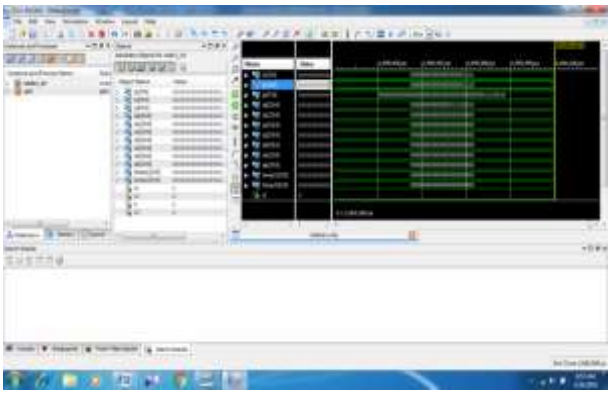

Fig -9: Simulation result of 24 bit IEEE754 multiplication using Urdhva Tiryakbhyam sutra

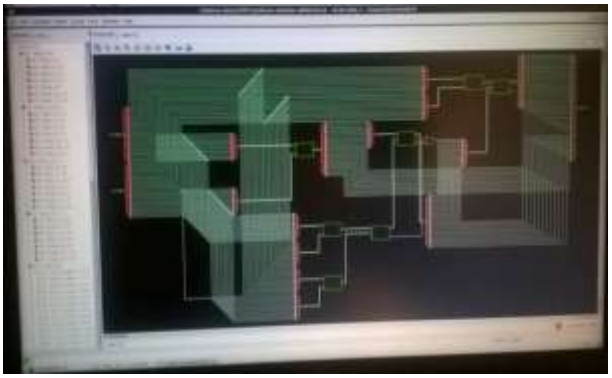

Fig -10: CADENCE Synthesis result of 24 Bit IEEE 754 multiplication using UT sutra

Table -1: Comparison of Results

Sl No:	Parameters of comparison	Xilinx Tool	Cadence
1	POWER	2977.50 µw	3977.507 nw
2	AREA	72 μm^2	12 μm^2
3	TIMING	8350 ns	5250 fs

6. CONCLUSION

This paper deals with the design of 24 bit Low power High speed floating point Vedic multiplier. The advantages of Vedic Multiplication over the conventional multiplication techniques are discussed. From the result we can find that the parameters like area, power, CPU speed consumed by Vedic multiplication technique is much less when performing synthesis using Cadence tool when compared to Xilinx synthesis. The proposed Vedic multiplication method is entirely different from conventional multiplication design. Here larger blocks are designed from the smaller blocks. The design and implementation difficulties for inputs of large number are decreased and modularity is increased. This will help in designing FFT structure. Urdhva Tiryakbhyam from Vedic Mathematics is a general multiplication formula that can be equally applied to all cases of multiplication. The conventional multiplication method needs more time & area on hardware than Vedic multiplication techniques. The most important matter is that performance speed is increased by increase in length of bit.

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BIOGRAPHIES

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