

Asymmetric Cascaded Half Bridge Multi Level Inverter with Permanent Magnet Synchronous Motor (PMSM)

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Abstract - In latest previous, countless multilevel architecture got here into existence. In this background, cascaded multilevel inverter (CMLI) is the promising structure. This kind of multilevel inverters synthesizes a medium voltage output centered on a sequence connection of vigor cells which use typical low-voltage aspect configurations. This attribute makes it possible for one to obtain high-fine output voltage and current waveforms. Nonetheless, when the number of phases rises switching components and the count of dc sources are also accelerated. This limitation grew to become a key motivation for the reward paper. In this paper, New uneven cascaded half of H bridge multilevel inverter with permanent magnet synchronous motor is proposed. It's pushed from the conventional asymmetric cascaded half H Bridge multilevel inverter. As a result, the proposed topology inherits its simplicity, flexibility and modularity in each building and control. The proposed topology switching pattern naturally reduces components voltage stress, switching losses and sooner or later decrees MLI dimension and fee. The validity of the proposed topology is validated with Matlab/Simulink design.

Key Words: Cascaded Multi level inverter, Total Harmonic Distortion (THD), Matlab/ Simulink.

1. INTRODUCTION

The future of energy electronic devices is motivated by attention that electrical energy needs to be stored by creating better energy transformation converters [1]. Conventional two stages H-link inverter produces regular volts similar to the referrals. However, its failures are too much [2,3]. Hence, multilevel inverters (MLI) are utilized to address these issues. The idea of multilevel converters has been presented since 1975. The normal use of a MLI inverter is to synthesize a preferred outcome volts from several feedback DC resources. The larger the stairway outcome volts stages the better the outcome volts quality is [2,4]. The normal types of MLIs are, Fairly neutral Point held NPC, Flying capacitor FC and Cascaded H bridge CHB [5-7].

Cascaded H-bridge MLI topology CHB is the most appealing topology in MLI. It is easy in development and control with variety of manipulate approaches [8,9]. CHB multilevel inverters attain bigger quantity of output voltage levels than twice the number of dc sources. Additionally, the series of H-

bridges makes modularized design and packaging. Even though CHB multilevel inverters have good modularity they use higher quantity of switching components and dc sources [4,6].

In Irregular configuration rate of DC currents for each H-bridge can be modified. For assume if feedback currents are modified in the rate of 1:2 and 1:3 then inverters will produce seven stage, 9 stage and 11 stage outcome waveforms respectively. But in this configuration more than one H-bridge is essential to generate resulting waveform. However, asymmetrical configuration can be provided by modifying the feedback currents to H-bridge. In this case, only one H-bridge is sufficient. Thus, many of modifying elements are reduced in order to obtain large amount of outcome stages.

On opposite, asymmetric MLI configuration are much extra efficient methodology to make use of DC sources. Non-equal DC sources V_{dcn} are utilized rather of equal ones in symmetric configuration. This gives more flexibility in combining different values of V_{dc} sources to one another.

Consequently, it produces extra output voltage levels with the equal quantity of utilized V_{dcn} and switches compared to symmetric procedure in identical MLI configurations [10, 12].

2. ASYMMETRICAL CONFIGURATIONS OF CHB INVERTER

Asymmetrical configuration with symmetrical output voltages across each H-Bridges:

The DC voltages of the H-bridge power cells introduced in the preceding section are all the same. Alternatively different dc voltages may be selected for the power cells [14]. Fig. 2(a) is constructed with unequal dc voltages, but of integer multiples magnitude dc sources. A switching scheme is implemented that renders an equal voltage stepped waveform. With $(m-1)/2$ number of dc sources m levels are achieved and $(m-1)$ numbers of odd harmonics are eliminated. Consequently, a number of sources required are halved.

Conversely, Fourier expansion of equal voltage steps is given by the following:

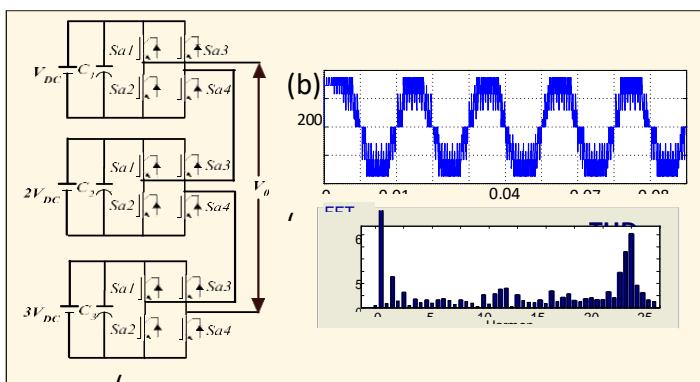


Figure 1.(a) Asymmetrical thirteen-level CHB inverter, (b) simulation verification of thirteen-level CHB multilevel inverter, (c) FFT spectrum

Thus, with the help of switching scheme, a number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This permits more voltage steps in the inverter and thereby yields improved voltage waveform for the same number of power cells. In the present structure the dc voltages for *H*-bridges are chosen as V_{DC} , $2 V_{DC}$, and $3 V_{DC}$ respectively. The three-cell inverter leg is able to produce thirteen level voltage waveform; that is, voltage waveform constitutes $6V_{DC}$, $5V_{DC}$, $4V_{DC}$, $3V_{DC}$, $2V_{DC}$, V_{DC} , 0 , $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, $-4V_{DC}$, $-5V_{DC}$, and $6V_{DC}$. Simulation and FFT results are shown in 1(b) and (c).

2.1 Asymmetrical configurations with asymmetrical output voltages:

In preceding section, asymmetrical configuration is introduced, but output voltages produced across each H-bridge are in symmetric in nature. It is also possible to develop an asymmetric configuration with asymmetrical output voltages. This control strategy allows us to generate large number of output levels

Proposed CMLI using sub-multi cells:

2.2 Proposed asymmetrical multi-cell CMLI:

The suggested irregular multi-cell CMLI includes n equivalent non-isolated dc volts resources which are used to synthesize a multilevel outcome volts by indicates of energy digital changes. The changes used in the topology are of two kinds. Some of them have to prevent both beneficial and negative voltages and perform the present in both guidelines. Therefore, these changes must be bidirectional. The other changes have to hold up against volts only with a specific polarity so that they are unidirectional. When a variety of dc resources per each basic cell (n) = 1, 2 then

unidirectional changes are sufficient to perform the function of suggested topology. But if $n > 3$ then bidirectional changes need to be integrated. Fig. 7 reveals the multi-cell configuration have only unidirectional changes since each sub-multi mobile comprises merely of two dc resources. Although the suggested configuration can be prolonged to several of volts stages, the changes T1-T4 have to hold up against a volts equivalent to the complete dc volts. This encourages to cascade the multi-cells so that the volts is distributed between the changes which makes it appropriate for greater volts programs, and the suggested sub-multilevel tissues produces the outcome volts of $2 N + 1$ stages. In the asymmetric multilevel inverter the value of the dc volts resources used in the different tissues is believed to be different so that more outcome volts stages can be produced using less changing gadgets. Assume that the p th mobile has up equivalent dc volts resources and consider the value of the first mobile dc volts resources to be as follows

$$V_{dc}; 1 \frac{1}{4} V_{dc}$$

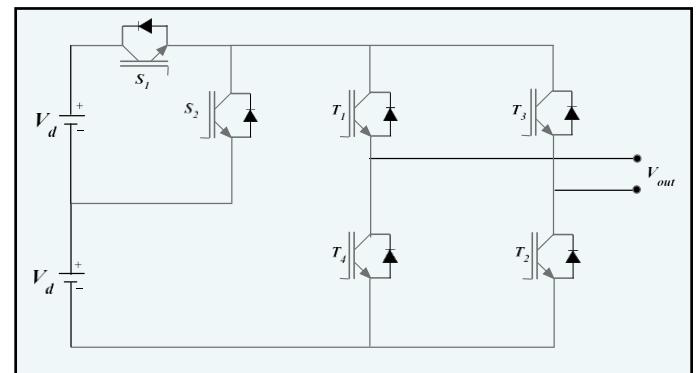
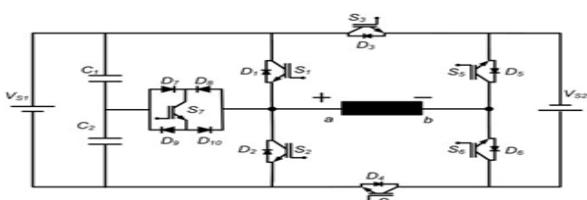


Figure 2 The proposed multi-cell CMLI.

3. EXISTING PROPOSED MLI TOPOLOGIES

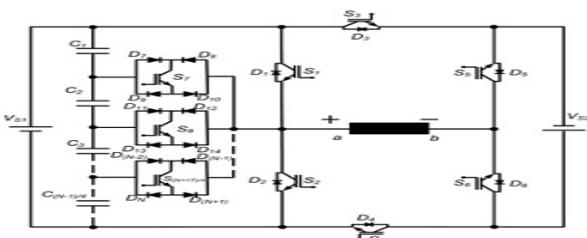
3.1. Proposed topology-I

The contract of Topology-I is verified in Fig. 3a. It contains of two DC volts resources VS1 and VS2, together with capacitors C1 and C2, which forms volts divider panel hobbies. An secure alternate is situated by managed trade S7 and four diodes D7, D8, D9 and D10 which is linked with HSC consisting by using six changes S1, S2, S3, S4, S5 and S6. When the values of the DC volts resources are similar, that is, VS1= VS2 then it may be often called symmetrical MLI otherwise irregular. Topology-I is able to provide 7/9/11level final result with distinctive mixture of DC volts useful resource at the same time integrating handiest seven managed alterations. The outcome volts stage with certain combination of DC volts resource is described in Desk 2. The overall method of the advised Topology-I is established in Fig. 3b.

Fig.3: Proposed Topology-I


(a) Circuit diagram of Proposed Topology-I for 9-level Inverter

3.2. Proposed Topology-II



(a) Circuit diagram of Proposed Topology-II for 9-level Inverter

Output levels, V	'ON' state switches	Conducting diodes
1	S_4, S_7	D_6, D_7, D_{10}
2	S_4, S_5	D_2
3	S_4, S_5, S_7	D_7, D_{10}
4	S_1, S_4, S_5	-
0	-	-
-1	S_3, S_7	D_5, D_8, D_9
-2	S_3, S_6	D_1
-3	S_3, S_6, S_7	D_8, D_9
-4	S_2, S_3, S_6	-

Table1. Different switching states for 9-level output

Components	Proposed Topology I	NPC	FC	CHB
Main power switches	6	16	16	16
Axillary switch	1	0	0	0
Diodes	10	72	16	16
Capacitors	2	8	36	-

Table2. Comparison of different 9-level inverter topologies for symmetrical MLI

The generalization of Topology-I in symmetrical configuration for N-level output is given as

Total number of controlled switches required =

$$(N + 19)/44 \quad (1)$$

$$\text{total number of diodes required} = (N + 1) \quad (2)$$

$$\text{total number of DC sources required} = 2 \quad (3)$$

$$\text{total number of capacitors required} = (N - 1)/44 \quad (4)$$

The settings of the suggested Topology-II are proven in Fig. 4a. It's adjustment of Topology-I within the light of generalization for symmetrical and uneven options. Topology-II contains of two secure changes linked with HSC from both the ends. The consisting alternate procedure is furnished by means of two DC volts useful resource along with four capacitors. The general framework of Topology-II is proven in Fig. 3b. It contains sequence relationship of a few essential tissues that can be managed for both formed and irregular options. Each and every cell contains eight managed changes, 14 vigour diodes, two DC resources and 4 capacitors. The DC resource on the left-hand part of HSC is distinctive as VL1, VL2, ..., VLn and on the right-hand a part of HSC is detailed as VR1, VR2, ..., VRn where n signifies form of sequence mobile phone. For shaped approach, the of DC resources are similar and for irregular approach, the of each DC assets are allotted in step with the three specific ways given in Desk 5. In common irregular CHB MLI principles of DC, assets are increased in either binary blend (2:1) or ternary blend (3:1). In nowadays released work of irregular settings of MLI elevated the volts fee as 4:1 in [30], 5:1 in [30] and 7:1 in [31]. The expand in rate of DC volts useful resource above the ternary blend displays almost certainly accomplishing larger variety of outcome degree with reduced form of changes in irregular settings. The one-of-a-kind mixtures of DC volts resource and corresponding effect phases are described in Desk 5. As a result, in the Topology-II a new standards of DC useful resource mixture (fourth criteria in Desk 5) is determined to get the bigger type of effect phases.

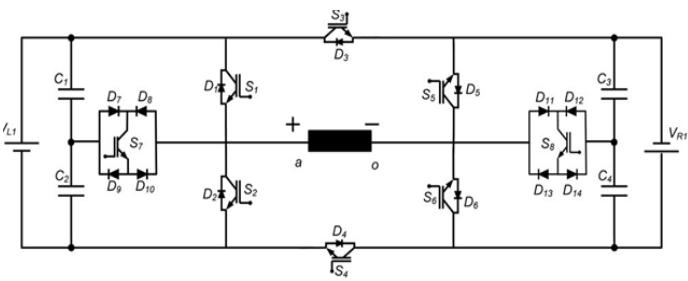


Fig.4: Proposed Topology-II

(a) Configuration of Proposed Topology-II

4. COMPARISON OF MLI AND SIMULATION RESULTS OF EXISTING TOPOLOGY

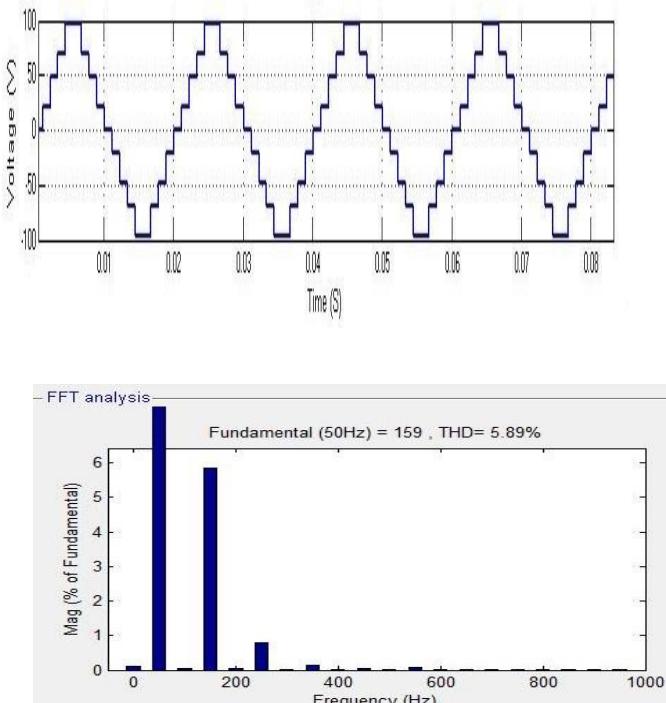
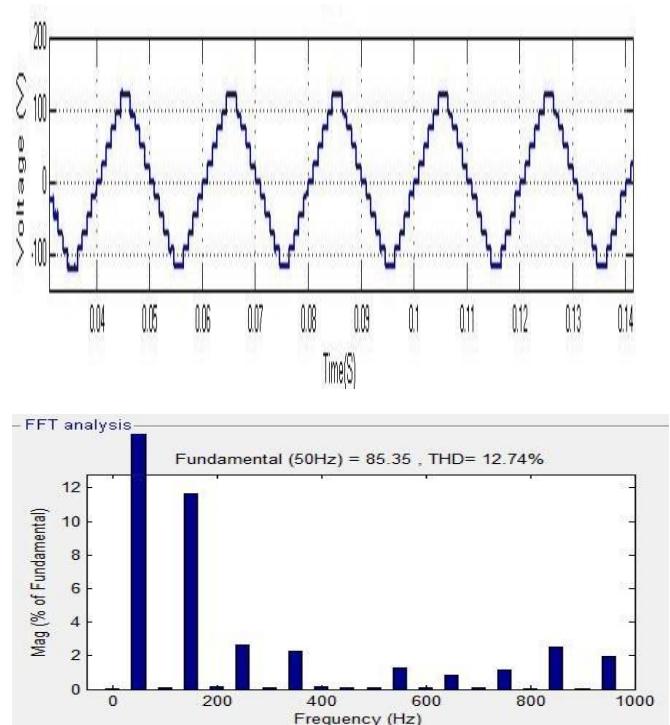
4.1 Comparison for symmetrical and asymmetrical MLI:

The topology-I is used for low and medium voltage applications. In comparison of other topologies the switches, diodes, capacitors and DC voltage sources also less. Consequently, cost, complexity, size of topology-I is reduced. This can limits their high -voltage applications.

The topology-II is used for high voltage applications. Which can also reduce the switch count compared to topology-I. Topology-II requires least number of IGBTs when compared to other topologies. The high levels of symmetrical and asymmetrical MLI are mathematically analyzed by using Fourier series transformation.

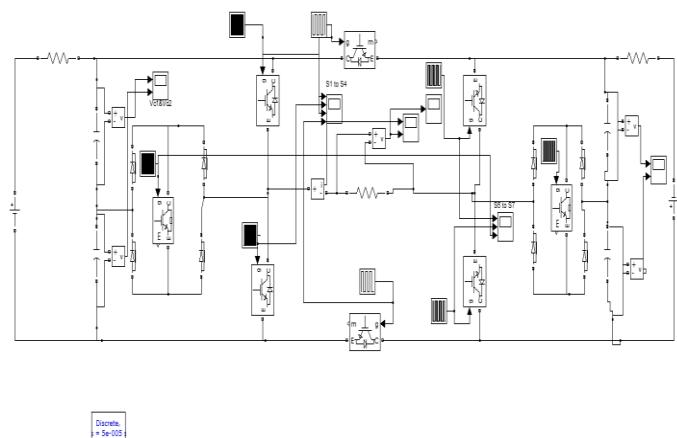
4.2. Simulation Results for Existing Topology:

To examine the performance of the proposed topologies simulation has been carried out using MATLAB/Simulink. Topology-I is simulated for symmetrical and asymmetrical configurations as 9-level and 11-level inverters, respectively. The simulation result for 9-level and 11-level inverters and their corresponding THD is shown in Figs. 5a,5b and 6a,6b.


Fig:5 Output voltage and corresponding THD for 9-level MLI

Fig:6 Output voltage and corresponding THD for 11-level MLI

NEWLY PROPOSED TOPOLOGY:

Topology-II is simulated in asymmetrical configuration to obtain 17-level output. The simulation result for 17-level inverter and their corresponding THD is shown in Fig 7a,7b.



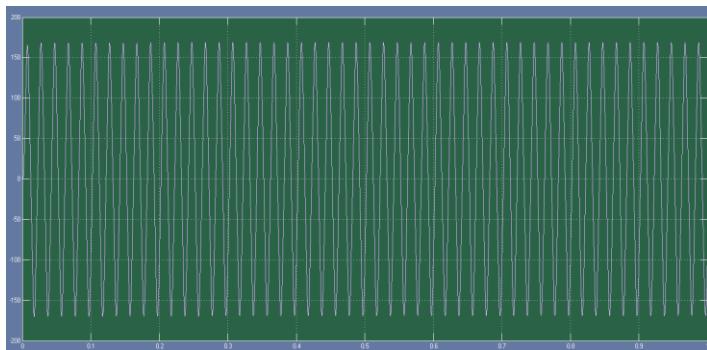


Fig.7(b).Output voltage for 17 level inverter

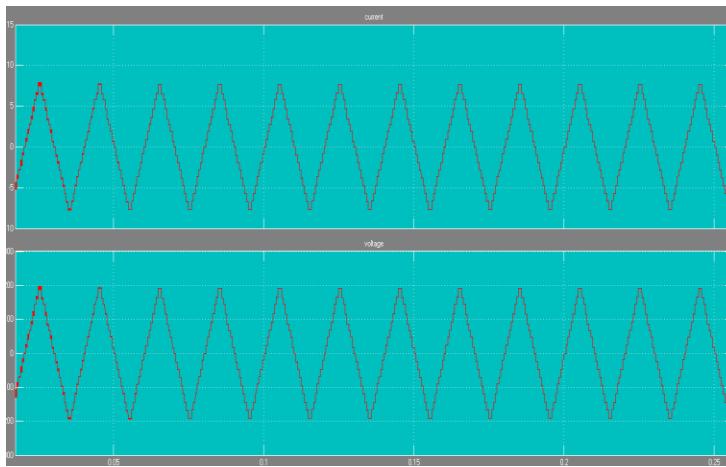
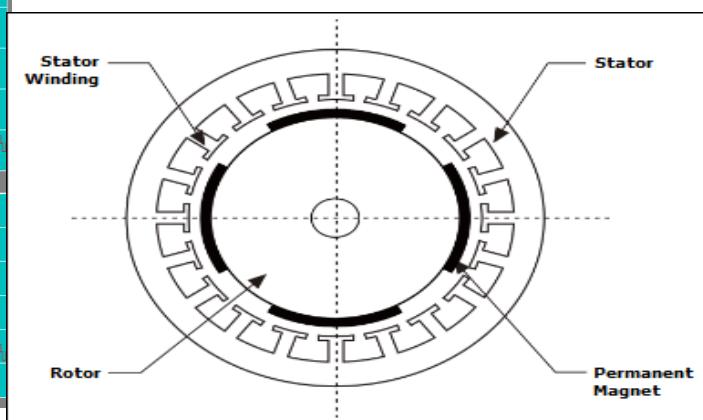


Fig.7(c) Output Voltage and Current waveforms for 17 level inverter

Among the various management techniques, SVPWM (Space Vector Beat Size Modulation) with PI current operator is commonly used for twisting management over PMSM due to a great management performance. A PMSM uses permanent heat included in metal blades to create a continuing magnetic area. The stator provides windings linked with an AC SUPPLY to generate a ROTATING MAGNETIC FIELD.

The settings of recently suggested topology are proven in fig. The irregular 17-level multilevel inverter can be choosing for the PMSM generate as a fill. The corresponding features of PMSM generate and total harmonic distortions also noticed, by using MATLAB/Simulink.



A permanent magnetic synchronous engine (PMSM) is an engine that uses long lasting heat to generate the air gap permanent magnetic area rather than using electromagnets. These engines have significant benefits, gaining the interest of scientists and industry for use in many programs. Two options of permanent magnetic synchronous engine pushes are usually considered based upon on the back-EMF waveform: sinusoidal kind and trapezoidal kind. Then different management techniques (and management hardware) are applied. In this paper, a management for the sinusoidal PMS engine is described.

The Simulation parameter values of 17-level asymmetrical multilevel inverter can be indicated in below table-3. PMSM have delay angles for switching ON and OFF purpose. i.e. 0° , 120° , 240° respectively.

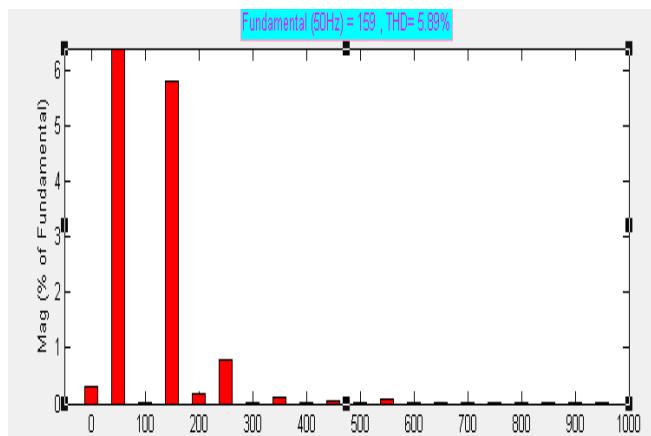
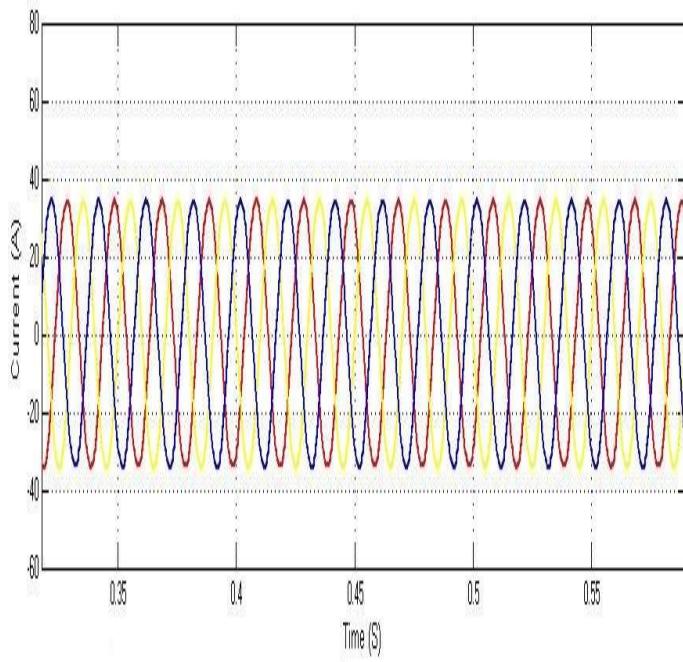
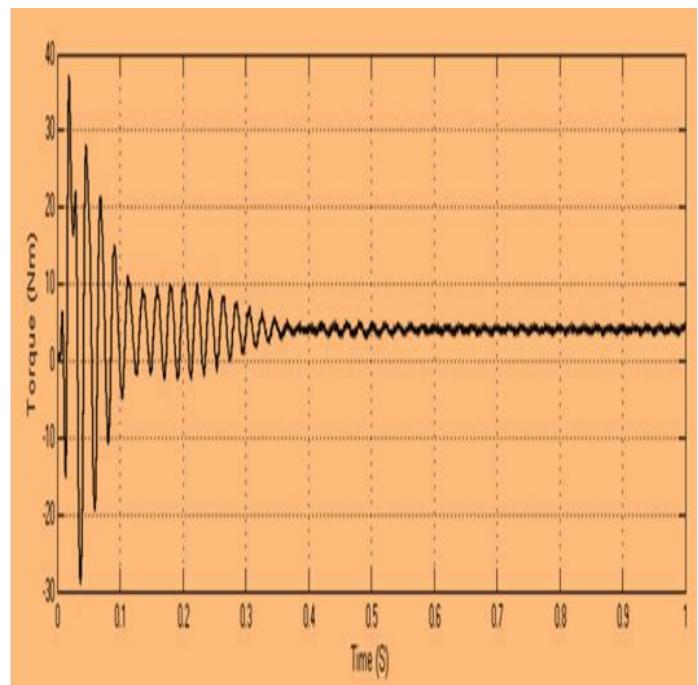


Fig.7.(d) Corresponding THD for 17-level MLI

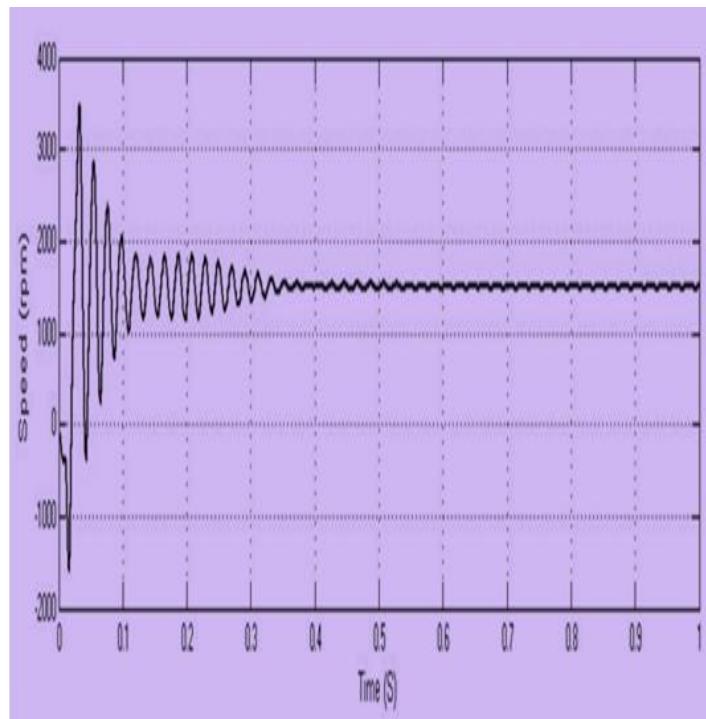
5. NEWLY PROPOSED TOPOLOGY WITH PMSM DRIVE

PMSM (Permanent Permanent magnetic Synchronous Motor) is much used in commercial programs, equipment for the home and software system due to the best quality, great twisting and great management performance. In order to get an excellent twisting management performance, many techniques are examined.

Parameters	17-level
Source-I	2V
Source-II	6V
Capacitors , μ F	1100
R, Ω	10
frequency, Hz	50

Table: 3. Simulation parameter values**OUTPUT WAVEFORMS:****Fig: 9.** Current output waveform of PMSM drive**Fig : 11.**Torque Output Waveform of PMSM drive**6. CONCLUSION**

Multilevel inverter has many advantages, for instance: price, dimension, complexity can be reduced. Moreover, it also minimizes on THD and increases the performance, certainly centred upon on the topology of formed and infrequent configurations of MLI. In this papers infrequent configurations of MLI with complete, as PMSM is recommended. The performance of the PMSM is finally verified through simulation.

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