An Analysis of CMOS based Low Power 2:4 Decoder at 32nm node using LECTOR Technique

Rajbeer Singh[1], Manoj Kumar Bandil[2]

[1]PG Scholar, Department of Electronics & Communication, ITM Gwalior, India
[2]Assoc Professor, Department of Electronics & Communication, ITM Gwalior, India

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Abstract:- As the speed of shrinking and speed of operation of devices has escalated day by day more and more functions are required to be embedded in a tiny piece of chip. Already power hungry circuits need extra power to diminish their requirement especially the portable ones. As the voltage of operation is diminishing which leads to rising of static power consumption due to rise in threshold leakage current caused by reduction of threshold voltage. A new technique known as LECTOR technique has been implemented which can be used to decrease leakage power without increasing overall dynamic power. LECTOR technique provides better option than other alternatives due to its effectiveness in active and idle state. In this work we have designed CMOS 2:4 decoder with Lector Technique which significantly reduces the leakage power and improves the performance of circuit in terms of power. We have worked on 32 nm node technology using 0.7V supply voltage with the help of SPICE simulation tool.

Keywords - CMOS, 2:4 decoder, Leakage power, leakage current, LECTOR etc.

I. INTRODUCTION

As the electronic industry is booming at an explosion rate the most advanced devices does not get limited to hands of some of the professionals or elite class of the society. Now everyone in the modern society from a kid to elderly people holds an electronic device and the devices are becoming more and more portable to make its availability convenient. High Power dissipation affects the battery life of portable device and hence the reliability, packaging and heat sink costs. Hence power consumption is a major issue to address in modern scenario of electronics [1]. The main types of power dissipation along with their origins are stated as:

- Dynamic power consumption which occurs when signals go through their transition due to switching on and off of CMOS device.

- Short Circuit power consumption which occurs when CMOS makes transition and both NMOS along with PMOS conduct simultaneously due to existence of conducting path between voltage supply and ground for a fraction of time.

- Static power consumption: It is the leakage current which consists of:

a) Reverse Bias diode leakage current which occurs due to reverse biasing of drain and source to well junctions.

b) Sub threshold leakage current is the current between source and drain of a transistor when transistor is in sub threshold region which is gate to source below the threshold voltage.

c) Gate oxide tunneling leakage current prominent in nanometer scale which occurs due to tunneling of carriers from bulk and source/drain overlap region through the gate oxide potential into the gate .

d) Gate induced drain leakage are the tunneling based leakage currents prominent in nanometer scale caused where the gate overlaps the drain.

e) Gate leakage current due to hot carrier effect prominent in nanometer scale which is due to drift over time of threshold voltage in short channel devices [2], [3].

Fig. 1 shows projections of the power consumption components of various years according to the International Technology Roadmap for Semiconductors (ITRS).This projection clearly shows that as devices get scaled down to nanometer scale static power consumption is expected to surpass the dynamic power consumption. All the above mentioned mechanisms of static power leakage, subthreshold leakage current are a major contributor in static power as the supply voltage has been scaled sown to keep dynamic power consumption within limit [4], [5]. But to maintain high drive current capability threshold voltage has to be scaled   which results in exponential increase of subthreshold leakage currents [6].

▲   **Energy per (W/L gate=3) Device Switching Transition**

◆   **Dynamic Power Dissipation per (W/L gate =3) Device**

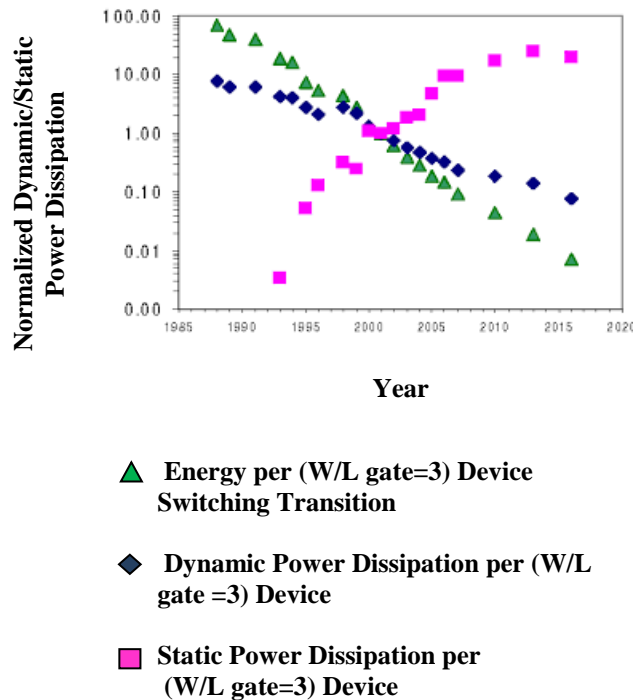■   **Static Power Dissipation per (W/L gate=3) Device**

Fig.1. Projection of the Power Consumption Component of various years [7].

In this paper we are studying the circuit of CMOS based 2:4 decoder using a new power saving technique. Decoder are the integral parts of all the processing chips as they are used as address decoders in memory systems, instructional decoders in CPU and also to activate particular set of output according to input data combination as in binary decoders. Decoders have basically input as the counter output which transits to activate a particular set of outputs. These outputs of decoder can be used to set particular device ON or OFF and can be used as clocking signals. These are widely used in memory systems of computer where they address the particular memory location depending upon the instruction by CPU [8]. Hence designing a power saving decoder has an impact on every device in the digital universe as decoders are integral devices of digital systems. A 2:4 Decoder has 2 inputs and 4 outputs along with an Enable signal. We analyse the parameters leakage current, propagation delay and leakage power of the proposed circuit along with the conventional CMOS circuit.

II. LECTOR TECHNIQUE

Scaling of technology following Moore's Law is not a straight line as various trade-offs are to be made between dynamic power consumption, static power consumption, propagation delay, area and cost has to be made. As the devices are becoming more and more portable so the requirement of power efficient devices is increasing day by day as the end of day it all depends on the battery life of devices. Static/Leakage power dissipation is the main culprit as it eats the battery even when the device is not in use.

In the proposed work we have used a technique known as LECTOR (Leakage Control TransistOR) which significantly reduces the static power consumption without influencing the dynamic power consumption

[9].The basic idea behind this technique is [10], [11] to have "A circuit with more than one transistor is off between power supply to ground having less leaky than a circuit with only one transistor is off between power supply to ground" [12]. We are showing LECTOR technique for general CMOS based gate circuits which consists of PUN (pull up network) and PDN (pull down network).This technique can be extended to any CMOS based gate circuit. In this circuit we have used two leakage control transistor (LCTs) between pull up network and pull down network [13] such that one of LCTs is always near its cut off region of operation. As LCT1 (PMOS) and LCT2 (NMOS) are introduced between nodes N1 and N2.Both the drains of LCTs combined to form output of CMOS circuit and their sources are connected to nodes N1 and N2 .Gates of both LCTs are cross coupled to the source of other LCTs. Voltages at the nodes N1 and N2 control the switching of both the LCTs. This feedback connection is such that whatever is the input at the gate, one LCTs is always near the cut off region. These are designed in such a way that these are self controlled LCTs requiring no external circuit to control them. Hence two LCTs increase the resistance between V_{dd} and ground reducing the leakage current. This technique is superior to other power saving techniques such as power gating, sleepy transistor, zigzag technique [14],[15],[16] etc as it does not require external circuitry to control them .The CMOS based Gate with LECTOR technique is shown in Fig. 2.
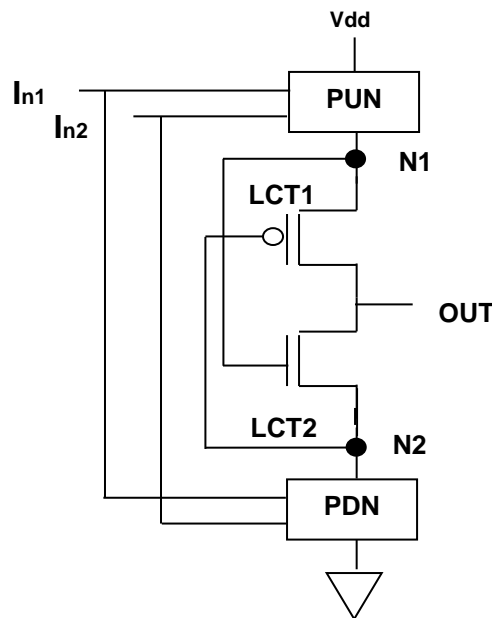

Fig. 2.LECTOR based CMOS Gate

III. PROPOSED CIRCUIT

We have proposed 32 nm based CMOS 2:4 decoder using LECTOR technique.2:4 Decoder is a basic decoder which can be used to build higher order decoders and it consists of two NOT gate and four AND gates. We have introduced two LCTs transistor in each pull up network (PMOS) and pull down network (NMOS) .The proposed circuit is shown in the Fig. 3.
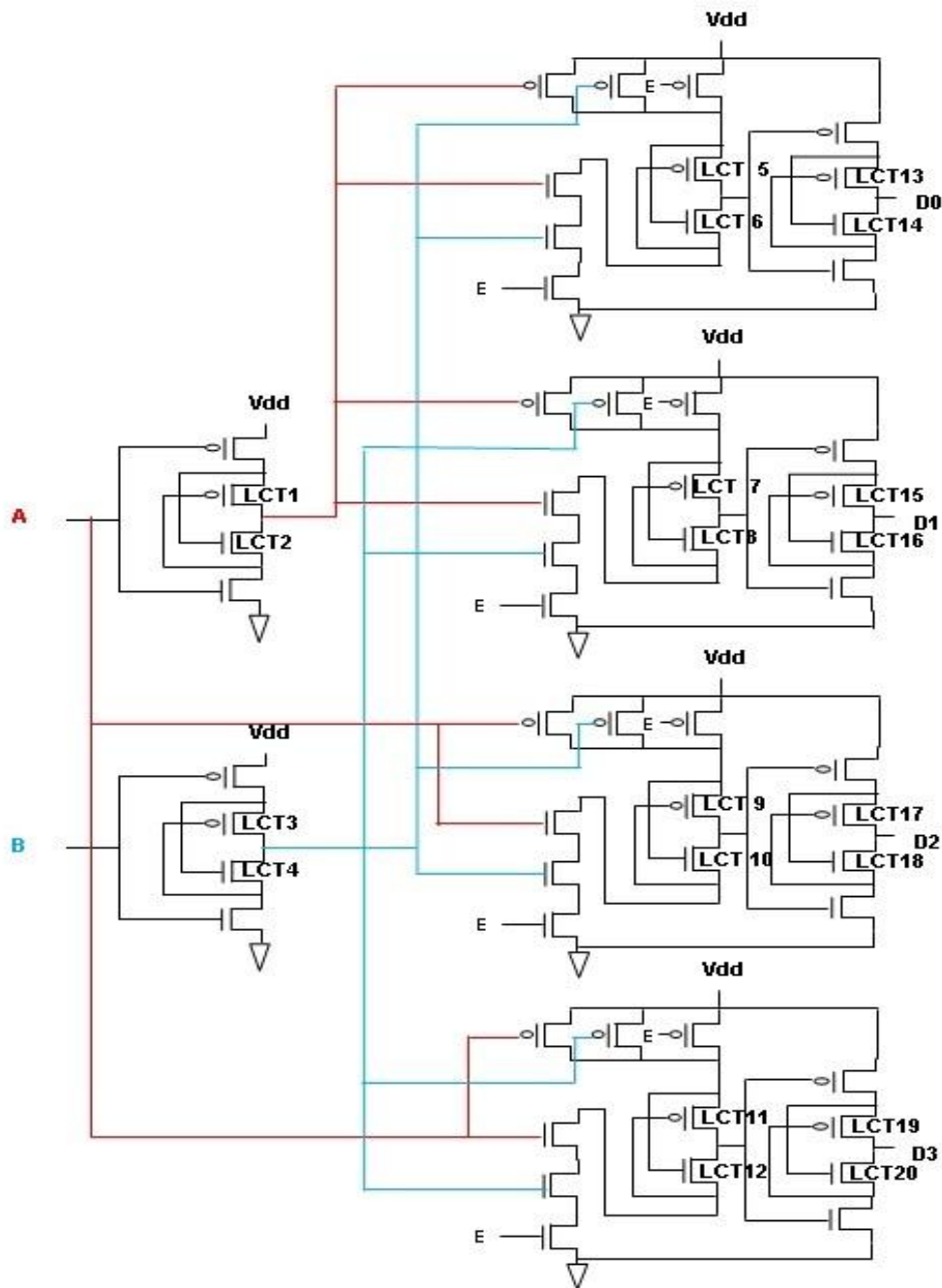
Fig.3. LECTOR based 2:4 CMOS Decoder

IV. RESULTS AND SIMULATION

The proposed LECTOR based 2:4 Decoder circuit was simulated using SPICE tools in 32 nm technology. Fig. 4 shows the output file of SPICE tool which reflects leakage power and leakage current of the circuit under study. Fig. 5 shows the waveform obtained at the output which is in agreement of the input combinational data. In Table 1, we have made comparison of power dissipation, leakage current and propagation delay between CMOS based conventional 2:4 Decoder and LECTOR based 2:4 Decoder. Fig. 6 shows the graphical representation of the decrease in power dissipation and leakage current along with increase in propagation delay. It is evident from the results that LECTOR based 2:4 Decoder shows improvement over CMOS based conventional 2:4 Decoder in terms of leakage power.

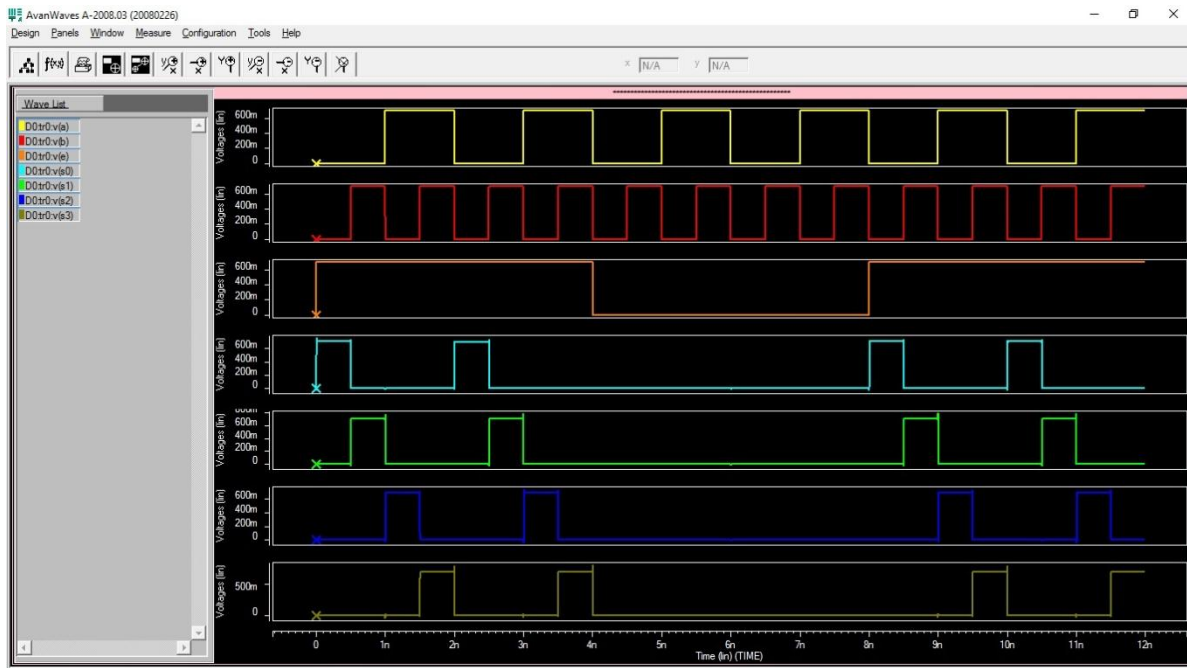Fig.4. Output File of SPICE Tool of LECTOR based 2:4 Decoder

Fig.5. Output Waveform of LECTOR based 2:4 Decoder

Table 1: Comparison of Parameters of Conventional CMOS based 2:4 Decoder and LECTOR based 2:4 Decoder

Parameters	CMOS based 2:4 Decoder 32nm	LECTOR based 2:4 Decoder 32nm	% Decrease in the Leakage Power	% Increase in the Propagation Delay
Supply Voltage	0.7v	0.7v	--	--
Leakage Power	331.0987nw	115.0931nw	65.23%	--
Leakage	472.9981nA	164.4188nA	65.23%	--

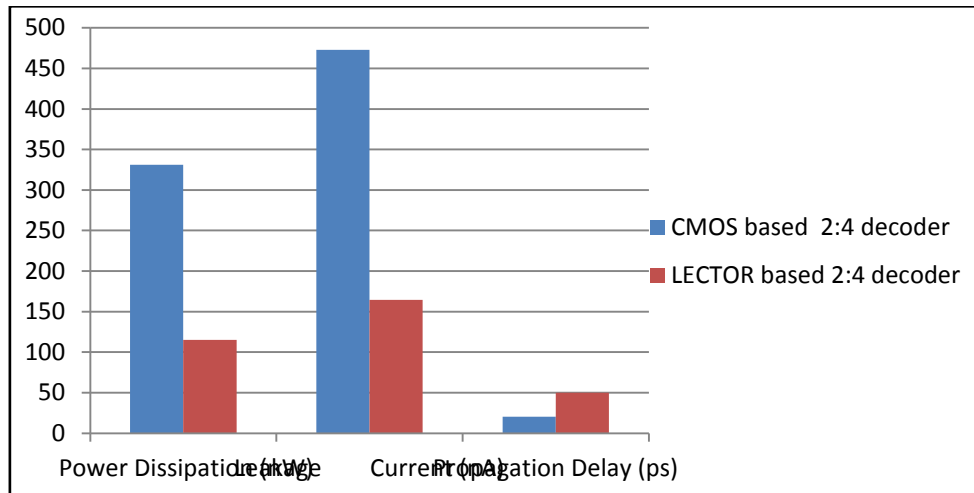| current				
Propagation Delay	20.390ps	50.120ps	--	145.81%

Fig.6. Bar Graph showing reduction in Power Dissipation and Leakage Current

V. CONCLUSION

In this paper we have proposed CMOS based 2:4 decoder using LECTOR technique and the results we obtained after performing simulation on 32 nm scale using SPICE tool are satisfactory. We have observed that power dissipation and leakage current has reduced by using LECTOR technique as compared to conventional CMOS 2:4 decoder outperforming the rise in propagation delay. There is a 65.23% of improvement in power dissipation of LECTOR based 2:4 Decoder as compared to conventional CMOS which overshadows the 145% increase in propagation delay. LECTOR technique can be applied to complicated circuits where power efficiency plays a major role. As we have performed simulation on 32 nm scale which can be extended to 22nm scale and further down the nanometer scale to find the effect of LECTOR technique in controlling the leakage power.

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