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Arithmetic logic Unit Design with Comparison Power Consumption on Different Foundries using Microwind Tool

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Abstract - : In this paper, An ALU design and implementing using different foundries like 50nm, 70nm, 90nm and 120nm. The performance of developed ALU analyzing and comparing in terms of area and power. The schematic of ALU circuit designing using DSCH 3.5 and its equivalent layout creating using Microwind tool.

Keywords: ALU, Foundries, Area, Power, DSCH, MicroWind Tool

1. INTRODUCTION

In Present era, as the technology is growing more and in terms of IC design, more number of transistors getting packed into an IC, which increases the size and total area in any physical design of device. So, at present, scaling is important for designing any device. So, other than Very large scale integration, there will be a existence of Ultra large scale integration technologies, for faster operation.

Major challenge is microscopic issues as ultra-high speed power dissipation and supply rail drop growing importance of interconnect noise, crosstalk reliability, manufacturing clock distribution. Low power also leads to smaller power supplies, less exclusive batteries, and enables products to be powered by signal lines (such as fire alarm wires) lowering the cost of the end result. The arithmetic logic unit (ALU) is the core of a CPU in a computer. The adder cell is the basic unit of an ALU. The constrictions the adder has to satisfy are area, power and speed requirements.

2. METHODOLOGY

2.1. ALU Design with Power Consumption

The ALU receives the information from the registers and performs a given operation as specifies by the control. A very simple ALU design, the control unit is made up of 4-1 multiplexer. The operation part consists of four kinds follows: and, or, addition and subtraction. The 'and' and 'or' operation are realized by using the basic logic gates. The addition and subtraction are realized using the ADDER user symbols. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits .A digital multiplexer made from MOS device selects one of the 4 operations results and directs it to a single output line. The full adder performs the computing function of the ALU. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three key in or input bits. It consists of three inputs and two outputs. Arithmetic functions like as addition, subtraction, multiplication and division are some examples.

The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices [2]. The power consumption in a CMOS digital circuit can be calculated using Eq.1. Whether it is a general-purpose system or an application specific processor, addition is by far the most frequently used operation.[4]

$$P = f'C.Vdd^2 + f'Ioff .Vdd + Ioff .Vdd \quad (1)$$

ALU truth table

Control		Select points	Result	Carry out
F1	F0			
0	0	Pass	A	0
0	1	Add	A+b	Carry from a+b
1	0	And	A • b	0
1	1	Not	A'	0

Now drawing the Schematic diagram of 1 bit ALU using DSCH-3.5 EDA tool will result in the gate level implementation of the circuit as in Figure.1 and Figure.2

3. SCHEMATIC AND LAYOUT

The schematic and layout of 1 bit ALU in DSCH schematic is designed. An arithmetic logic unit, or ALU (sometimes pronounced "Al Loo"), is a combinational network that implements a function of its inputs based on either logic or arithmetic functions. ALUs are at the heart of all computers as well as most digital hardware systems. The arithmetic and logic unit (ALU) performs all arithmetic operations (addition, subtraction, multiplication, and division) and logic

maneuvers. Logic operations test various conditions encountered during processing and allow for different actions to be taken based on the results. The data required to perform the arithmetic and logical functions are inputs from the designated CPU registers and operands. The ALU relies on fundamental items to perform its operations.

The schematic design using different symbols from libraries and connect it.Making Verilog File and save it. Then compile Verilog file in Microwind tool and generate layout.

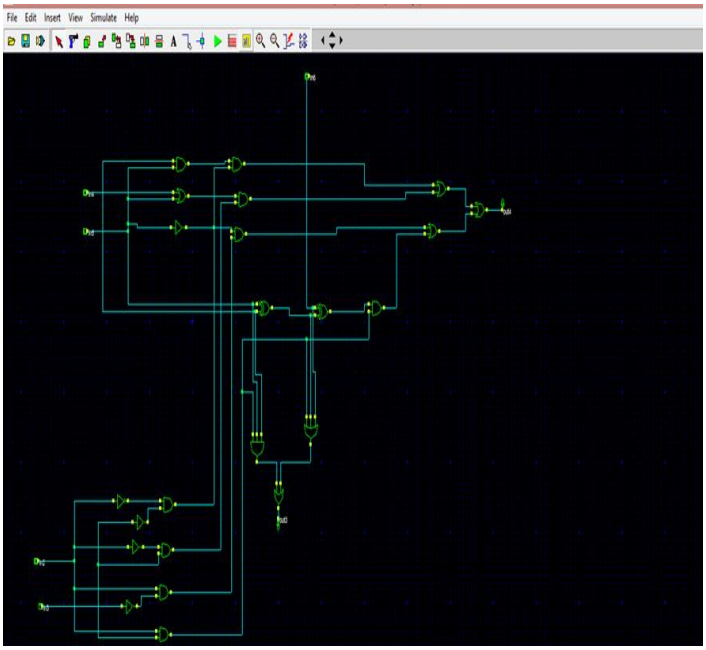

Fig 1. Schematic Diagram of 1 Bit ALU

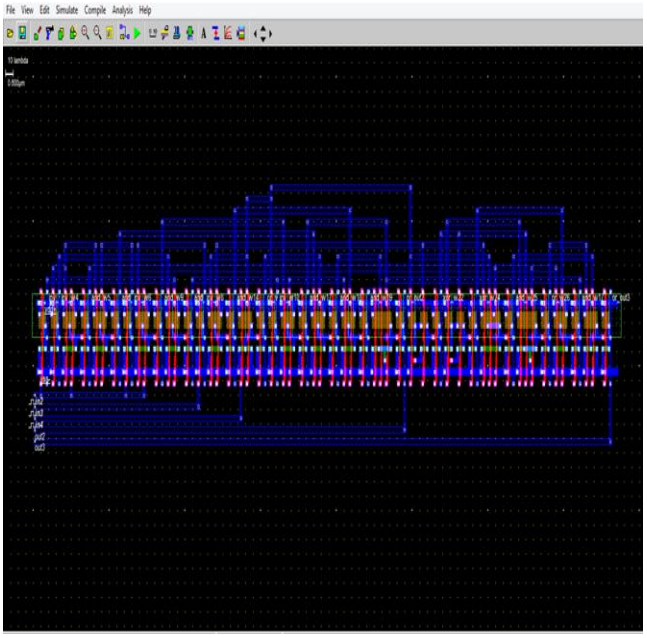

FIG. 2 Layout of 1 Bit ALU

4. SIMULATION AND RESULTS

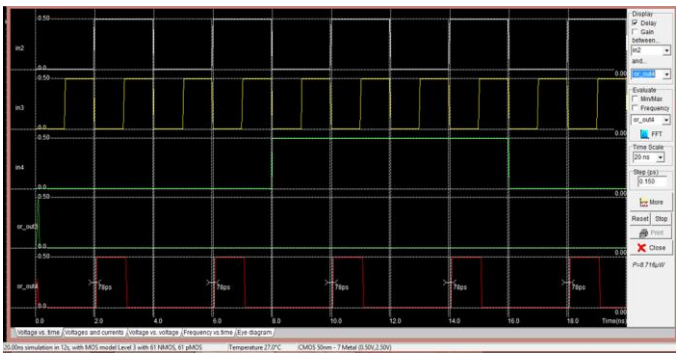

Fig. 3 Simulation of 1 bit ALU in 50 nm

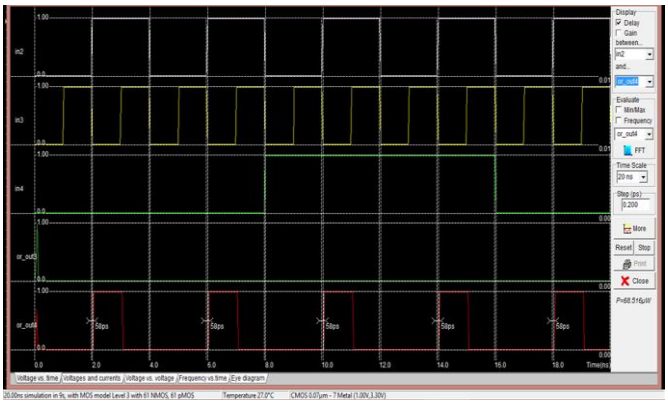

Fig. 4. Simulation of 1 bit ALU in 70 nm

Table -1: Comparative Different Foundries with Power Consumption

Different Foundries	Power Dissipation
50 nm	8.716µW
70nm	68.516µW
90nm	62.19µW
120nm	97.466µW

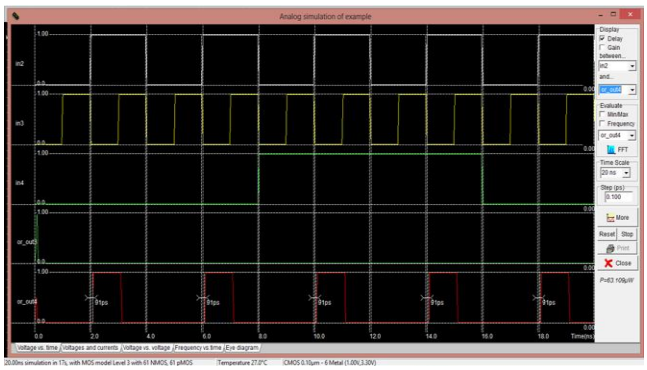

Fig. 4 . Simulation of 1 bit ALU in 90 nm

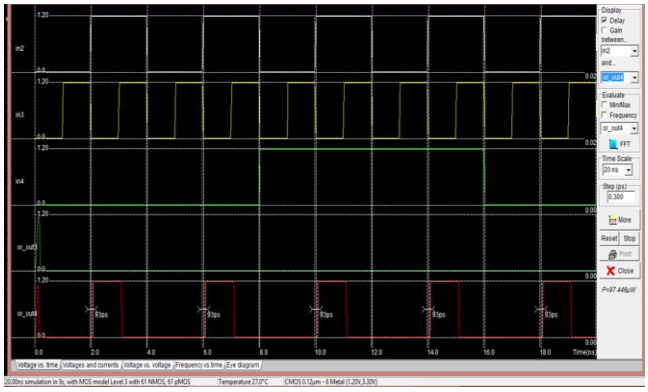

Fig. 5 Simulation of 1 bit ALU in 120 nm

5. CONCLUSIONS

The schematic design using different symbols from libraries and connect it. Making Verilog File and save it . Then compile Verilog file in Microwind tool and generate layout and simulate in different foundries.

The comparison of different power dissipation as shown in table 1. A comparative study of the silicon area and the power consumption has been done in the circuit using different channel lengths such as 50nm, 70nm, 90nm and 120nm. The circuit is designed and simulated using DSCH schematic tool and the layout is developed by Microwind VLSI CAD Tool. The designed circuit has shown a remarkable reduction in the consumed power of 90% in 50nm foundry as compared to 120 nm foundry

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