

A STUDY ON THE LEAKAGE MECHANISM OF STANDARD 6T SRAM CELL

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ABSTRACT: Static Random Access Memory (SRAM) continues to be critical components across a wide range of microelectronics application for consumer wireless to high performance server processors, multimedia and System on Chip (SoC) applications. As the technology scales down to 130nm and below, the leakage power of SRAM is becoming one of the most critical concerns for low power applications. Thus minimizing the leakage current, improving read and write stability are major challenges in the emerging technologies. The leakage currents of standard 6T SRAM cell are studied. The 6T SRAM cell suffers from problems like write delay, less static noise margin, read stability and high-power dissipation.

Keywords

SRAM, Leakage current, CMOS, Gate Leakage, Subthreshold leakage.

1. INTRODUCTION

In modern System on Chips (SoCs) almost 30% of total chip power consumption is due to memory circuits. As the sizing of the SRAM is in nanometre scale, variations occur in parameters like threshold voltage, oxide thickness and doping concentration. These variations in turn result in various types of leakages which have to be minimized. The gate leakage current and sub-threshold leakage currents are the dominant leakage components in deep sub-micron technology (100nm – 35nm). Due to the fast growth of battery-operated portable devices like cell phones, laptops, and tablet PCs, there arises a demand for low power devices. To address this challenge of power

saving, researchers in the domain have reported work at the device level, circuit level, architecture level, and algorithm level. The power reduction techniques have been classified into two categories. They are the leakage control in the standby mode and leakage control in the active mode. In the standby mode, at the circuit level techniques, it cut off the circuit from the power supply

rails while in the active mode, certain design modifications, alongside adding additional transistors are used to minimize the leakage current during run time. Process, supply voltage and temperature are the major challenges in designing high performance systems.

2. RELATED WORKS

In most of the electronic system memories are a core part. Performance regarding speed and power dissipation is the major areas of concern in memory technology. Sah et. al (2015) proposed SRAM cells based on 6T, 7T, 8T, and 9T configuration are compared on the basis of performance for read and write operations. Analysed results show that the power dissipation in 7T SRAM cell is least among other configuration due to the usage of single bit for both read and write operations. Among different studied SRAM configuration, this SRAM cell also provides the least power delay product. In 90nm CMOS technology, the performance in terms of power dissipation and power delay product are slightest for 7T SRAM cell among the other SRAM configuration.

Jawar Singh et. al (2008) proposed a novel 6T single ended SRAM cell for ultra-low power applications. The design has a strong 2.56 x worst case RSNM compared to standard 6T SRAM cell. A strong ability of logic 'one' is achieved, which is problematic in a Single ended-SRAM cell with 36% improvement compared to standard 6T SRAMs. The dynamic and leakage power dissipation are reduced by 28% and 21% respectively as compared to standard 6T SRAM cell. The cell has better noise margin and it is highly tolerant to process variations. However, it is less vulnerable to noise and suffers from high write delay.

Garima Upadhyay et. al (2017) proposed a method to achieve 8x and 6x time enhancement in leakage current and power dissipation respectively compared to conventional 6T SRAM cell. Simulations results show improvement in read stability read/ write delay, ION/IOFF, leakage current and power dissipation

using 32 nm technologies. But for various technologies the leakage current may increase.

2.1 Leakage Mechanisms

Dinesh Chand Gupta and Ashish Raman (2012) focused on leakage current minimization in single static random-access memory (SRAM) cell in 90nm complementary metal oxide semiconductor (CMOS) technology. The leakage current mainly consists of sub threshold leakage current and gate leakage current in 90nm CMOS technology. So, minimizing the sub threshold leakage current and gate leakage current is most important aspect in low power memory design. A technique based on dual threshold voltage (V_t), dual gate oxide thickness (t_{ox}) and dual power supply (V_{DD}) assignment together to minimize gate leakage and sub threshold current of SRAM cell. Simulation results using 90nm CMOS technology shows that this technique can reduce the total leakage current dissipation of a single SRAM cell by more than 75% with less delay penalty. Meenakshi et. al. (2013) stated that the supply voltage is scaled down, the transistor threshold voltage is also scaled to maintain performance. As a result of the low threshold voltage, leakage power increases rapidly due to the exponential relationship between leakage and V_t . Leakage can be reduced by using higher- V_t transistors, but by using an all high- V_t transistor cell performance degrades by an unacceptable margin. Parimaladevi Muthusamy and Sharmila (2016) shows that leakage current measurements made on hold mode of operation have 40.63 nano amperes. The different leakage current of standard 6T SRAM cell in standby mode is shown in Figure 1.

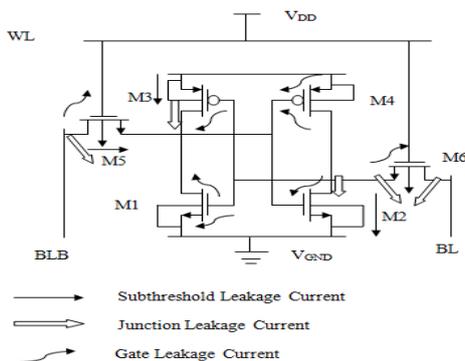


Figure 1: Leakage currents of 6T SRAM cell

2.1.1 Reverse Biased Junction Leakage

Through the reverse biased diodes, the junction leakage occurs from the source or drain to the substrate when a transistor is in the OFF mode. A reverse-biased p-

n junction leakage has two main components, one is because of minority carrier diffusion/drift near the edge of the depletion region and the other is because of electron-hole pair generation in the depletion region.

2.1.2 Gate-Induced Drain Leakage

The Gate Induced Drain Leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. The significant band bending in the drain allows the electron-hole pair generation through avalanche multiplication and band-to-band tunneling in a nMOS transistor with grounded gate and drain potential at V_{DD} . Since the holes are rapidly swept out to the substrate a deep depletion condition is created and at the same time, electrons are collected by the drain resulting in GIDL current.

2.1.3 Gate Direct Tunneling Leakage

The gate leakage flows to the substrate from the gate through the “leaky” oxide insulation. Oxide layers thicker than 3–4nm results from the Fowler-Nordheim tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. For lower oxide thicknesses (which are typically found in 0.15 μ m and lower technology nodes), however, the leading effect is direct tunneling through the silicon oxide layer. Direct tunneling mechanisms include Electron tunneling in the Conduction Band (ECB), Electron tunneling in the Valence Band (EVB), and Hole tunneling in the Valence Band (HVB), amid which ECB is the dominant one.

2.1.4 Subthreshold Leakage Current

The Subthreshold Leakage Current is the drain-to-source leakage current when the transistor is in the OFF mode. When the applied gate source voltage is less than the threshold voltage of the transistor, i.e., weak inversion mode this will happen. Subthreshold current flows due to the minority carriers diffusion current in the channel of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). At the same time as the supply voltage (V_{DD}) is being uniformly scaled down with successive technology nodes. The transistor delay is inversely proportional to the difference of supply and threshold voltage, the threshold voltage must also be scaled down proportionally with each technology node to maintain the circuit performance. This leads to an exponential increase in subthreshold leakage current. Increasing the threshold voltage (V_t) of the transistor is an effective way to reduce subthreshold leakage.

2.2 Leakage Reduction Techniques

The requirement of low power is becoming a major problem in high performance systems such as microprocessors, DSP's etc. Neerja Singh et. al. (2017) focus on the comparisons of various leakages current reduction techniques in SRAM cell. With continuous technology scaling leakage current has become the biggest challenges of VLSI industries. With projected large memory content of future systems on chip, it is important to consider the leakage current in SRAM as it has been the driving force behind the rapid development of CMOS technology.

3. CONVENTIONAL 6T SRAM CELL

A standard 6T SRAM bit cell is shown in Figure 1 has two identical CMOS inverters connected in a loop of positive feedback. It forms a basic unit, that is, a flip-flop. The internal nodes of the bit cell always contain complementary values. The cross coupled inverter pair itself consists of two PMOS pull-up devices (M3 and M4) and two NMOS pull-down devices (M1 and M2). Two NMOS pass gate or access devices (M5 and M6), which are controlled by the word line (WL), serve as switches between the inverter pair and the complementary values. The cross coupled inverter pair itself consists of two PMOS pull-up devices (M3 and M4) and two NMOS pull-down devices (M1 and M2). Two NMOS pass gate or access devices (M5 and M6), which are controlled by the word line (WL), serve as switches between the inverter pair and the complementary pair of bit lines (BL, BLB) also called data lines, used to read in or write to the bit cell. The data in SRAM bit cell is stored as long as the power is maintained to the bit cell. The read and write operations in a standard 6T SRAM bit cell are performed in the following ways.

3.1 Read Operation

By inserting the WL signal, the read operation will initiate. It connects the internal nodes of the cell to the pre-charged BLs. Then, depending on the internal nodes voltage, one of the BLs will develop some differential voltage with respect to the other one. Figure 2 shows the waveforms of 6T SRAM cell during read operation. In this Figure, BL will remain at its pre-charged value while BLB will be discharged to a lower level through transistor M2 and M6. Because of the voltage divider formed by the M2 and M6, there is degradation in the value of node B which should be kept below the switching threshold of M1-M3 inverter to prevent non-destructive read operation.

3.2 Write Operation

Figure 3 shows the waveform of 6T SRAM cell during write operation. At the beginning of write cycle BL is pre-discharged to 0V while BLB is pre-charged to V_{DD} . By asserting the WL signal the write cycle begins. By pulling down the value of the internal node the new logic value can be only written that is initially '1'.

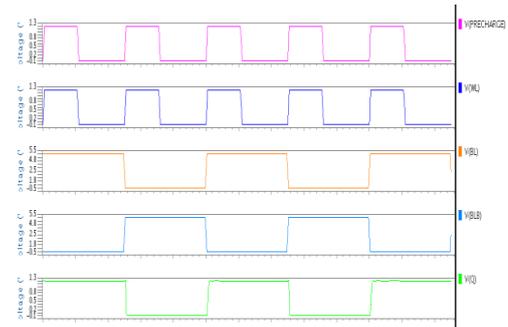


Figure 2: Six Transistor SRAM cell during read operation

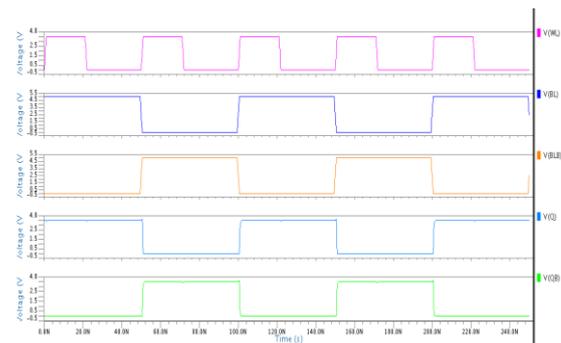


Figure 3: 6T SRAM cell during write operation

For read data stability, the node B voltage cannot be higher than ΔV . Because of the current that passes through transistors M3 and M5 to the BL, the voltage at node A will decrease until it reaches the switching threshold voltage of inverter M2-M4. To ensure reliable write operation the voltage at node B should be pulled down to a level lower than V_t .

From the above-mentioned implications of non-destructive read operation and reliable write operation, it is obvious that there is a trade off in sizing of access transistors in order to satisfy these requirements. For read operation they need to have high ON resistance while they require low ON resistance for write operation. This trade off can be alleviated by choosing minimum width for access transistors (M5 and M6), minimum width for pull-up transistors (M3 and M4) and larger than minimum width for driver transistors (M1 and M2).

4. DISCUSSION AND RESULTS

The leakage currents of conventional 6T SRAM cell are analyzed at 27°C temperature and tabulated in Table 1. From the tabulation it is analyzed that the gate leakage current (I_G) of standard 6T SRAM cell is 17.125 nA and the subthreshold leakage current (I_{SUB}) of 6T cell is 29.86 nA.

Table 1. Leakage current (in nA) of conventional 6T SRAM are analyzed at 27°C temperature.

| TRANSISTOR | CONVENTIONAL | |
|------------|---------------|-------------------|
| | I_G (nA) | I_{SUB} (nA) |
| M1 | 0.7 | 7.85 |
| M2 | 4.12 | 1.79 |
| M3 | 6.70 | 0.7 |
| M4 | 3.48 | 19.32 |
| M5 | 0.275 | 0.1 |
| M6 | 1.85 | 0.1 |
| TOTAL | 17.125 | 29.86 |

5. CONCLUSION

The conventional 6T SRAM cell suffers by larger leakage current. Also, the read/write delay, read stability and write-ability of the standard 6T cell must be improved. From the study, gate leakage current is 17.1nA and the subthreshold leakage current of 6T cell is 29.86nA. Subthreshold leakage current is more than the

gate leakage current. Alternative bitcell approaches can be adopted for reducing subthreshold leakage current.

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