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# Reduction of Power, Leakage and Area of a Standard Cell ASICs using Threshold Logic Flip Flops and Power Gating Techniques

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**Abstract -** *In this paper, a new approach to reduce dynamic power, leakage, and area of standard cell ASICs, without sacrificing its performance is described. The approach is based on designing a threshold logic gates (TLGs) and its integration with the conventional standard-cell design flow. The threshold gate behaves as a multi-input, single- output, edge triggered flip-flop, which computes a threshold function of the inputs on the clock edge. The function realized by a given threshold gate is determined by how signals are mapped to its inputs. Here pulsed inputs of varying width are provided at the input. The resulting circuits, with both conventional and TLGs (called hybrid circuits), are placed and routed using commercial tools. Here the tool used is Tanner tool v13. The power gating techniques is used along with threshold logic gates to reduce the leakage and dynamic power dissipation. This power gating method along with TLF improves the area and power of the ASIC circuits. The proposed circuit is designed in 45nm technology. A significant reduction in power, leakage, and area of the hybrid circuits when compared with the conventional logic circuits is observed.*

***Key Words***: MTCMOS, Threshold logic Flip flop (TLF), Power Gating Techniques.

## 1. INTRODUCTION

The demand and popularity of portable electronics is driving designers to strive for smaller silicon area, higher speed, longer battery life and more reliability. Power is one of the premium resource a designer tries to save when designing a system. In every circuit, power dissipation occurs. It is not possible to eliminate it completely but the amount of dissipation can be reduced. Conventional ASIC design involves constructing network of CMOS logic gates to implement a given function. Low power Application specific integrated circuit (ASIC) design results in increased battery life and reliability enhancement. In this paper, a threshold logic gate methodology is used along with some power reduction techniques to improve the ASIC performance.

This methodology is based on the design of threshold logic gates and its integration with conventional standard cell design. Threshold gate is a multiple input, single output, edge triggered flip flop. This flip flop computes the threshold function of the inputs on the clock edge. The resulting circuit is a hybrid circuit which is the combination of conventional logic gates and threshold logic cells. By using this hybrid circuit, the power dissipation can be reduced compared to conventional designs.

First we have analysed the architecture and operation of basic PNAND cell. After that a new approach for computing threshold is implemented. Finally this new approach is combined with power gating techniques to reduce the dynamic and leakage power dissipation in the circuit. So the final design will have the combination of conventional standard cells (AND, OR, NAND, NOR) and PNAND cell.

## 2. THRESHOLD LOGIC FLIP FLOP

The fig-1 shows the basic schematic of threshold gate with k- inputs, referred to as PNAND-k cell. The circuit consists of three parts, namely, input network, sense amplifier and SR latch. The input network is divided into two networks namely Left input network (LIN) and Right input network (RIN). Both these networks are complement to each other.

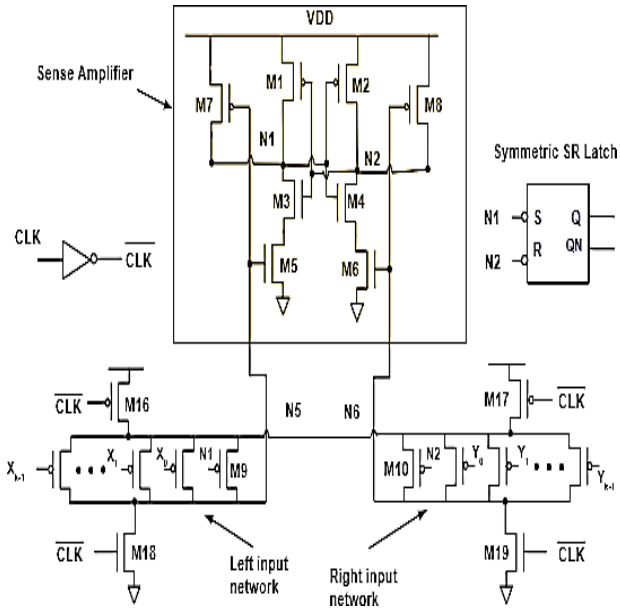


**Fig -1**: Basic PNAND cell

In the circuit, CLK is used as the reset pin. If CLK = 0, the circuit will reset. If CLK makes a change from 0 to 1, then the circuit will be enabled. The cell operates in two phases. One is the reset phase and the other is the evaluation phase. When CLK = 0, the circuit is in reset phase and when CLK changes from 0 to 1, it is in evaluation phase. So here the difference in conductivity between the two input network i.e. LIN (Left input network) and RIN (Right input network) is sensed and amplified. The greater the difference, the faster and more reliably the cell operates. The difference in conductance is mainly determined by the number of active devices in the input networks. Here in this basic PNAND cell, a signal assignment method called optical signal assignment is used to compute the threshold function of the given inputs. In the basic PNAND-k cell, the library of PNAND-k cells with k = 3,5,7,9 can realize 71 basic functions. By using the OSA method a set of valid threshold function can be generated for a given set of inputs.

### 3. A NEW APPROACH FOR TLF

For a threshold gate, here we are using the basic PNAND cell with a different logic method. Instead of using OSA method for computing the threshold function to realize a given functionality, a pulsed input of varying width is applied to the input network. This is due to the reason that when the threshold increases, the depletion width also increases and hence the leakage decreases and when threshold decreases, the depletion width decreases and therefore leakage increases. So in order to reduce the leakage, the threshold value need to be increased. This can be achieved by adjusting the access transistor in the input networks. By adjusting the access transistor, the threshold voltage can be varied.

### 4. POWER GATING TECHNIQUES

Power gating technique is one of the most efficient techniques used to reduce the power consumption. This technique is used in integrated circuit design to reduce power consumption, by shutting off the current blocks of the circuit that are not in use which means it transfers the energy to circuit only during the active mode and not in the standby mode.

There are a number of power gating techniques are exist but here in this paper only three such technique is considered, namely stack, sleep and MTCMOS techniques.

In sleep method the sleep transistor isolate the logic network and hence it reduces the leakage power during the sleep mode. The leakage power reduction in stack technique is achieved by splitting an existing transistor into two half size transistors. The Sleepy Stack Technique joins the Stack and Sleep systems. The current transistors splitted into two half size transistors in the Sleepy Stack system like as Stack procedure. Between the splitted transistors one of the sleep transistors will be placed in parallel. The leakage current is suppressed by the stack transistor and saves the state. While the sleep transistor will be off during the sleep mode. Sleep transistor is placed in parallel to the one of the stacked transistor and in active mode it reduces delay&resistance of the path.

So power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a circuit in

standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. Usually a high $V_T$ sleep transistors are used for power gating, in a technique also known as multi-threshold CMOS (MTCMOS). The sizing of sleep transistor is an important design parameter.

### 4.1. Circuit working using Power gating techniques

The circuit diagram incorporating the TLF and Power gating techniques is shown in Fig-2.

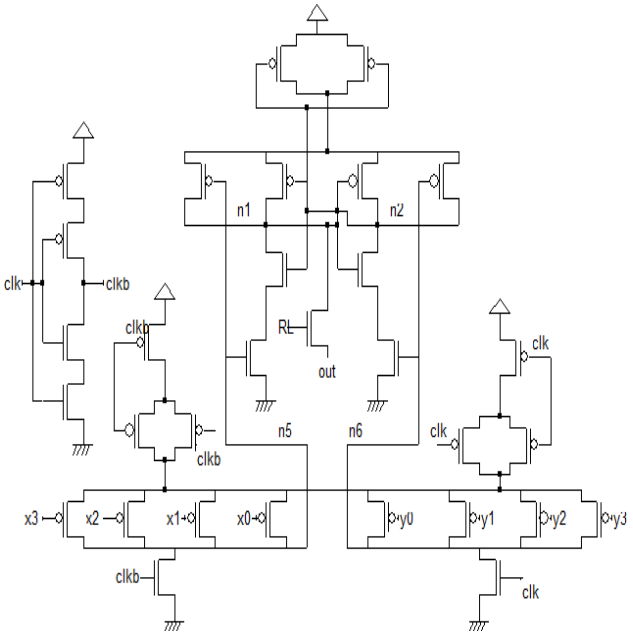


**Fig -2**: The proposed architecture

The sleep technique is applied at the CLK circuit. Here the header switch conducts only in the active mode which is used to reduce the leakage power dissipation. Footer switch conducts during the standby mode to reduce the dynamic power dissipation. By using MTCMOS technique, a boot up voltage is applied to the body bias terminal. It causes the threshold voltage to increases which helps to reduce the leakage power dissipation.

## 5. SIMULATION RESULT

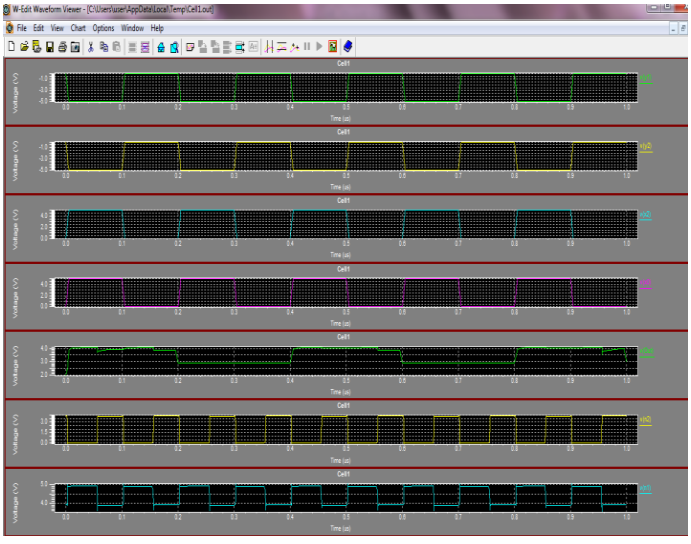

**Fig -3**: Simulation result for proposed design

**Table -1:** Result Comparison

| | Average power consumed (mW) | Technology Implemented |
|---|---|---|
| Conventional Threshold Logic Flip flop | 9.665 | 65 |
| TLF with Power gating Techniques | 2.65 | 45 |

## 6. CONCLUSION

In this paper, a new approach for power reduction in standard cell ASIC using a combination of conventional logic gate, threshold flip flop and power gating technique is described. It is observed from the output that the new approach consumes less power compared to the existing design and occupies less area without satisfying the speed. Use of power reduction techniques in TLF improves the performance of the overall circuit. A significant improvement in power, leakage and area were observed. About 73% power reduction is achieved in the proposed design. The proposed design can also be implemented using registers so that more data can be stored. Finfet and CNT can be viewed as the future implantation for this design for standard cell ASICs.

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