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RELIABILITY ENHANCEMENT OF LOW-POWER SEQUENTIAL CIRCUITS USING POWER GATING TECHNOLOGY

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Abstract – *This paper deals with low-power ASIC designs with power gating technology. They compromises with high performance and low area and power consumption, taking advantage of both latch and flip-flop features. While the circuit reliability and robustness against different process, voltage, and temperature variations are considered as critical issues with current technologies, no significant reliability study was proposed for traditional transmission gate pulsed latch circuits. In this paper, present a study on the effect of different PVT variations on the behavior traditional transmission gate pulsed latch circuits with power gating technology , while keeping their main advantages of high performance, low power, and small area. The proposed designs have negligible power overhead when running at nominal supply voltage, and they have higher yield per unit power when compared with the traditional design at different voltages and temperatures. The proposed circuit is implemented using Tanner v13 in 45 nm technology.*

Key Words: Pulsed latches, power gating techniques, low power, voltage scaling etc

1. INTRODUCTION

FLIP-FLOPS are considered the most popular sequential elements used in conventional ASIC designs. This is mainly because of the simplicity of their timing model, which makes the design and timing verification processes much easier. The high performance custom designs tend to use latches due to their lower timing in some designs. Although latch based designs are typically robust to clock skew and jitter (due to the latch transparency period), latches have a complicated timing model, which, in turn, complicates the design and the verification processes and increases the risk of hold time violations, especially with PVT variations. Pulsed latches have been always proposed to decrease power consumption and increase performance. In PLs with relatively wide pulse widths were used to allow cycle borrowing and tolerate any clock skew. In order, to compensate for any data before the end of the pulse. The structure of transmission gate pulsed latch is similar to differential latch structure, due to the presence of weak PMOS transistors in the master latch it is very difficult for the transition to take place when there is a change in input.

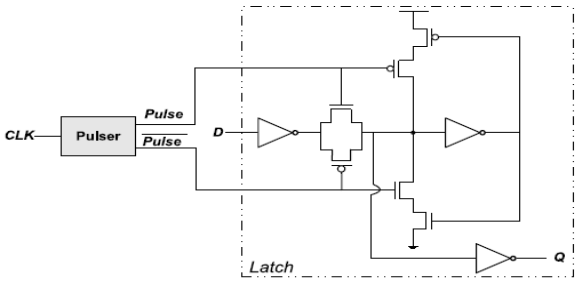

Fig -1: Simple diagram of a transmission gate pulsed latch

Pulsed latches are used in above figured; single pulser can be shared by more than one latch. The advantages of this circuit are area and power consumption savings.Pulser usage can eliminate the need for some of the clock buffers in the circuit.

2. Overview of Power Gating Technology

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing. Power Gating is effective for reducing leakage power. Power gating is the technique wherein circuit blocks that are not in use are temporarily turned off to reduce the overall leakage power of the chip. This temporary shutdown time can also call as "low power mode" or "inactive mode". When circuit blocks are required for operation once again they are activated to "active mode". These two modes are switched at the appropriate time and in the suitable manner to maximize power performance while minimizing impact to performance. Thus goal of power gating is to minimize leakage power by temporarily cutting power off to selective blocks that are not required in that mode.

2.1 Fine-grain power gating

Adding a sleep transistor to every cell that is to be turned off imposes a large area penalty, and individually gating the power of every cluster of cells creates timing issues introduced by inter-cluster voltage variation that are difficult to resolve. Fine-grain power gating encapsulates the switching transistor as a part of the standard cell logic.

Switching transistors are designed by either library IP vendor or standard cell designer.

The size of the gate control is designed with the worst case consideration that this circuit will switch during every clock cycle resulting in a huge area impact. Some of the recent designs implement the fine-grain power gating selectively, but only for the low threshold cells. If the technology allows multiple low threshold libraries, the use of low threshold devices is minimum in the design (20%), so that the area impact can be reduced. When using power gates on the low threshold cells the output must be isolated if the next stage is a high threshold cell. Otherwise it can cause the neighboring high threshold cell to have leakage when output goes to an unknown state due to power gating.

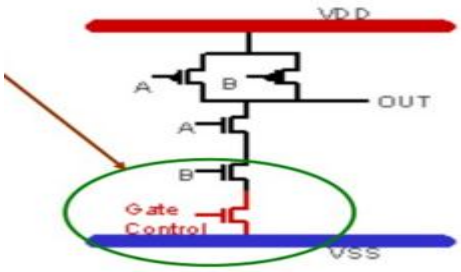

Fig -2: **Fine-grain power gating**

Gate control slew rate constraint is achieved by having a buffer distribution tree for the control signals. The buffers must be chosen from a set of always on buffers (buffers without the gate control signal) designed with high threshold cells. The inherent difference between when a cell switches off with respect to another, minimizes the rush current during switch-on and switch-off.

2.2 Coarse-grain power gating

The coarse-grained approach implements the grid style sleep transistors which drives cells locally through shared virtual power networks. This approach is less sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller area overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the power-gating transistor is a part of the power distribution network rather than the standard cell.

3. OVERVIEW OF ARCHITECTURE

The new architecture for transmission gate pulsed latch is designed by power gating technology. Here we used stack technique. In which the basic circuit is connected with both header an footer switches. The PMOS transistor is connected to the vdd. During active mode the header switch will be conduct and transfer the drain voltage to the given circuit. But in stand by mode it cannot work. So, that leakage power is reduced. The similar operation is carried out in footer switch, it will conduct on the stand by mode .The NMOS transistor is connected as a footer switch. Due to this power dissipation is grounded.

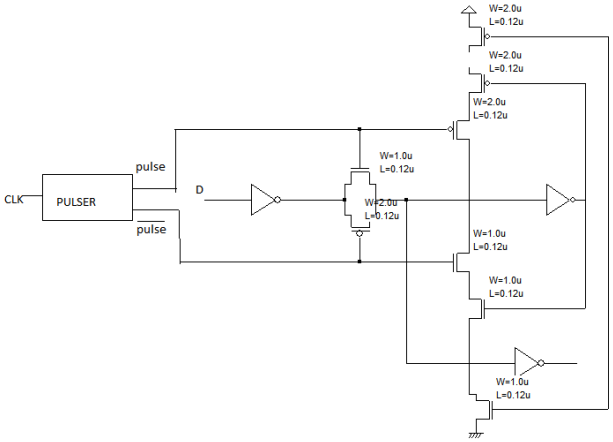

Fig -3 PROPOSED DIAGRAM

3.1 SIMULATION RESULT

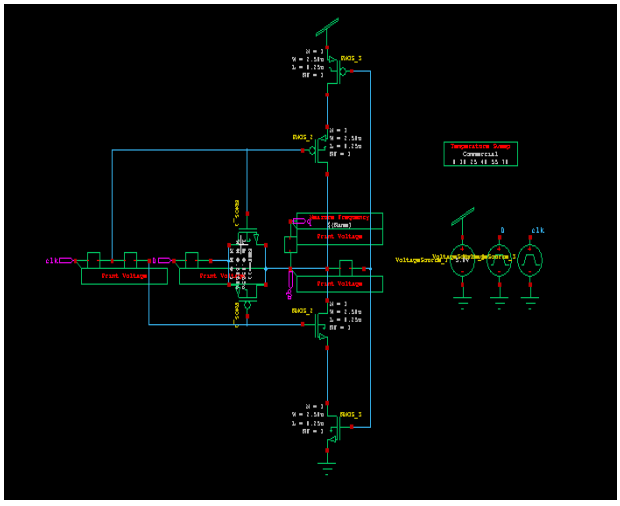

Fig -4:Simulation of proposed design

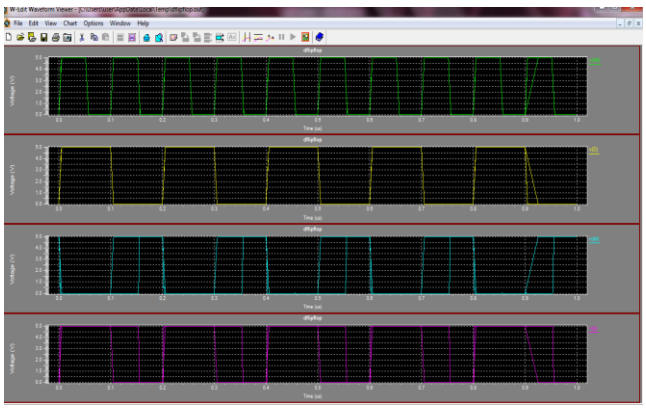

Fig -5:OUTPUT WAVEFORM

Table -1: Comparison Table

	Voltage (vdd)	**Power**	**TECHNOLOGY**
Traditional transmission gate pulsed latch	3v	4.27w	90nm
Proposed system	5v	2.204w	45nm

3. CONCLUSION

In this paper presented the effect of PVT variations on the pulsed latch performance in low power circuit. The circuit is implemented using Tanner v13 in 45 nm technology. The analysis considered both the pulser and the latch to evaluate the reliability of the entire pulsed latch circuit. In addition, the benefits of having a power gating technique were discussed. Stack technique is used in the proposed system to reduce power. Finfet and CNT can be viewed as the future implantation for this design for standard cell ASICs.

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