Comparative study of different AC-DC Converter for High Step Down

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Abstract - *In this paper a single stage three phase ac-dc converter using SiC MOSFET is compared with conventional two stage [Power factor correction (PFC) and dc-dc stage] ac-dc converter. In this model the dc-dc stage is not present. From the first stage (i.e PFC) high frequency pulsating voltage is given to a high frequency transformer, giving a condensed version. Adding to this there is zero voltage switching (ZVS) in the MOSFET present which is not there in the conventional model. A sine pulse width modulation (PWM) is applied to operate the switches. The main aim is to reduce the cost, increase the efficiency and power factor.*

Key Words*: *Power facto stage , Zero voltage switching, Pulse width modulation

1. INTRODUCTION

Three phase electric power is most commonly used to transfer electric power worldwide. It is used in power generation transmission and distribution. It is much more economical than a 2 wire single phase circuit at the same line to ground voltage since it uses lesser conductor material to transmit a given amount of electrical power. A front end ac-dc PFC stage is present so as to create sinusoidal currents, synchronized with corresponding phase voltage [1-3]. Boost derived topology is preferred due to its simple structure, low cost, and reliability. In many high power applications like in More Electric Aircrafts (MEA) it will have high loads but will be required to work in low voltages [8]. So for this to happen we need to step down the voltage to lower value using dc-dc converter. The common topologies for dc-dc stage are phase shifted full bridge type and resonant type (having L and C) [4-10]

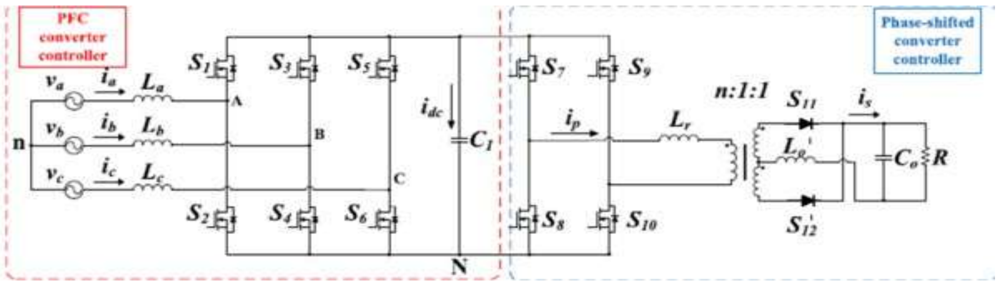


Fig:1a Circuit diagram of conventional ac-dc converter

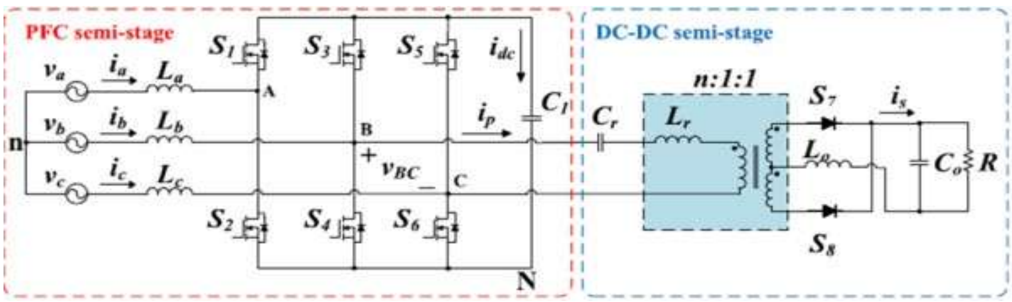


Fig:1b Rectified circuit diagram where transformer leads are connected to the source

In Fig 1a [1] conventional ac-dc converter is shown. it has 10 switches, where each switch has a separate gate driver circuit and heat sink attached to it. This is a major contribution to size, weight and cost. The dc link capacitor plays a major role to limit the dc voltage ripple, which further adds to weight and cost.

In Fig 1b [1] the most of the challenges were rectified. the number of switches used are reduced thereby reducing the switching loss. The overall structure was made more simple compact and cheaper.

2. BLOCK DIAGRAM

As shown in the fig2 the main aim is to reduce the voltage from the main ac source which is at 415V and at a very high frequency 400Hz. This is then given to a PFC semi stage side.

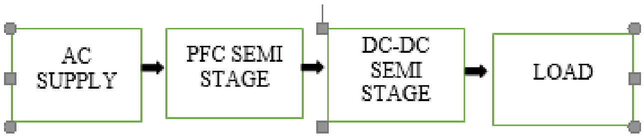


Fig2**:** The basic block diagram

Lr is the leakage inductance for the center tapped transformer with a turns ration n:1:1 which steps down the voltage and provides isolation. L_o and C_o performs as a low pass filter.

3. CLASSIFICATION OF UNIDIRECTIONAL THREE-PHASE RECTIFIER SYSTEMS

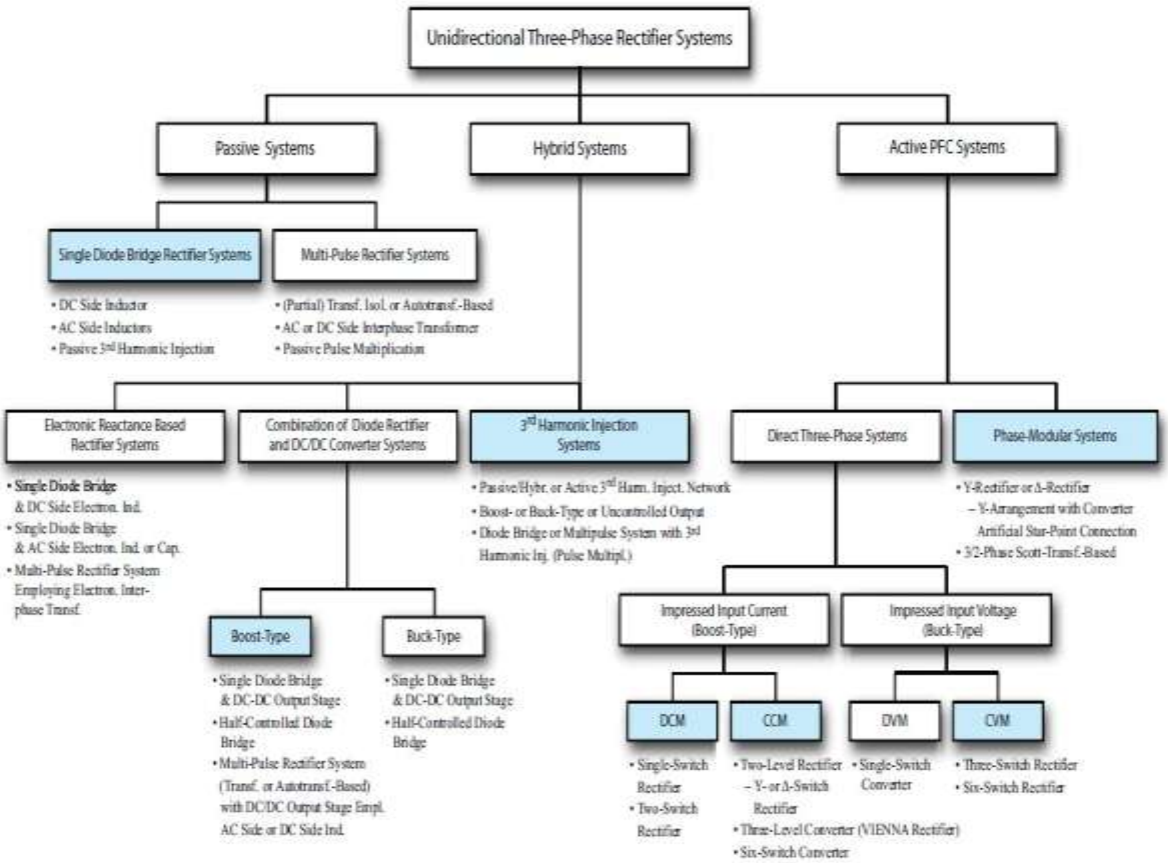


Fig3: Flow chart of different branches of three phase rectifier

In Fig. 3, a classification of unidirectional three-phase rectifier circuits is shown and has purely passive *systems* which:

1) contain no turn-off power semiconductors, i.e.;

2) work purely mains-commutated;

3) employ low frequency, i.e., passive components for output voltage smoothing and mains current shaping of several converter stages working in parallel or series [5].

4. PFC STAGE

PFC rectifier used in this paper tells about both sinusoidal and current regulation of the dc output voltage. It should be noted that an active harmonic filter with lower raring that is in parallel to a passive rectifier machine which will cause a sinusoidal mains current but the output voltage remains the same. Over lively filtering inspite of bigger implementation effort, PFC rectifier is frequently used due to the advantage of steady source voltage at load side [5].

5. PULSE WIDTH MODULATION

Recently the development and research of pulse width modulation rectifiers is increasing. The two most common faults are base drive and shoot through. Due to the problem caused by PWM, it can effect the equipment & in turn stop the manufacturing leading to financial loss. This is the main reason to have good fault tolerance & better reliability. Minimized three phase PWM rectifier supplied from unbalanced source storage.

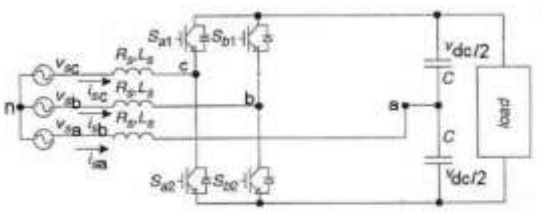


Fig 4: a basic circuit where the switches are controlled using PWM

The rectifier voltage vector is defined from line to neutral voltages V_{an} V_{bn} V_{cn} which can be calculated from V_a V_b V_c. They are the common pole voltages. Vo is the voltage between neutral point and midpoint of dc capacitor[4].

6. DC LINK CAPACITOR

A dc link capacitor is maninly used to link two sources. It s mainly connected positive to negative of a rectifier

The DC link should have following characteristics:

a) low voltage ripples

b) should not affect the performance of PF.

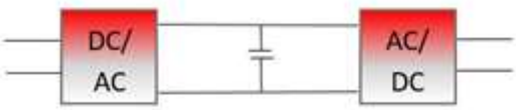


Fig5: Dc link capacitor used between converters

where its main objective is to increase the power factor and make it as close as unity. In the conventional method there is a large dc capacitance present which is further given to rectifier (specifically synchronization rectifier). And a transformer is connected where its input voltage is in relation to the dc capacitor. This is the main difference from the present model. Here the transformer is connected to the main source which in turn reduces the value of the dc link capacitor. Now this dc output voltage is reduced to a low voltage. In the PFC stage there are inductors in order to boost the input ac. There are complementary dead band present for the switches present in high and low voltage

7. ZERO VOLTAGE SWITCHING

For achieving ZVS at the lower load power, higher value of inductance is required in order to sink the enough energy from the parasitic drain-source capacitances to discharge them fully. Besides increasing the inductance value for ensuring ZVS, alternatively the switching frequency can be tuned to ensure ZVS at all switches. [7]

The main objective of tuning switching frequency at different load powers is to manipulate the phase lag of the net input impedance and ensure that it is inductive in nature. Therefore, it is necessary to investigate the equivalent input impedance of the PSFB converter.

8. MODELLING AND CONTROL SCHEME

The rectification can be done by unidirectional three- phase diode rectifiers with capacitive smoothing of the output voltage and inductors on the ac or dc side The low complexity and high robustness (no control, sensors auxiliary supplies, or electromagnetic interference (EMI) filtering) of this concept must, however, be weighed against the disadvantages of relatively high effects on the mains and an unregulated output voltage directly dependent on the mains voltage level. The mains behavior of a power converter is characterized, in general, by the power factor λ, and/or the fundamental current to voltage displacement angle Φ, and the total harmonic distortion of the input current

THDi which are related by the equation 4

$$\lambda=\frac{1}{\sqrt{1+THD_i{}^2}}\cos(\Phi) \qquad (4)$$

Due to sine pulse width modulation control the input voltage of the dc-dc semi stage has line frequency.

Due to this there will be a slow variation in output voltage. There is a second order LC filter to attenuate the lower frequency ripple, allows the high frequency component to pass through. The voltage drops at Lo and the current through output capacitor Co are both zero. Therefore, the equivalent input resistance of the secondary / tertiary sided would be R. after it is transferred to the primary side, the equivalent circuit of the dc-dc semi stage is then depicted in Fig 6.

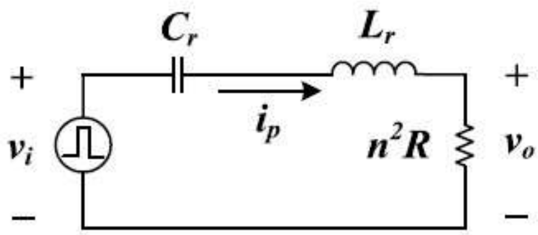


Fig 6 : LC circuit

By using the Laplace transform, the voltage transfer function is formulated in (6)

$$\frac{V_0}{V_i}=\frac{n^2R}{L_r}s/\left(s^2+\frac{n^2}{L_r}Rs+\frac{1}{C_rL_r}\right) \qquad (5)$$

This acts as a bandpass filter, the maximum gain is located at the resonant frequency

$$\omega_0=\frac{1}{\sqrt{L_rC_r}} \qquad (6)$$

and the quality factor is

$$Q=\sqrt{\frac{L_r}{C_r}}/(n^2R) \qquad (7)$$

The transfer function in (5) can be changed to (8) using w_0 and Q

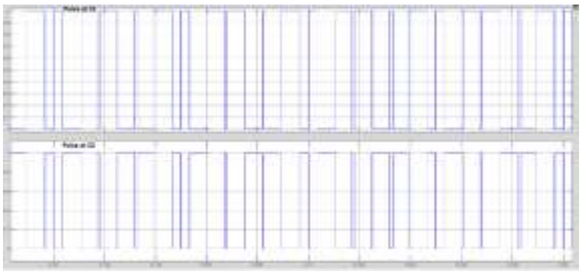
$$\frac{V_0}{V_i} = \frac{n^2 R}{L_r} s / \left(s^2 + \frac{n^2}{L_r} Rs + \frac{1}{C_r L_r} \right) \quad (8)$$

9. COMPARISON WITH THE CONVENTIONAL METHOD TO THE PROPOSED MODEL

It is found that in the conventional circuit the harmonic distortion was above 12% , while in the present and more compact circuit the harmonic distortion has bee reduced to a value 10%.

As the harmonic distortion is reduced, also the efficiency has been increased to a value close to 95%.

10. SIMULATION RESULTS



Time

Fig 7: pulses from the PWM

In this figure as u can see the PWM outputs are obtained. A sine wave taken from the source is compared with a high switching frequency.

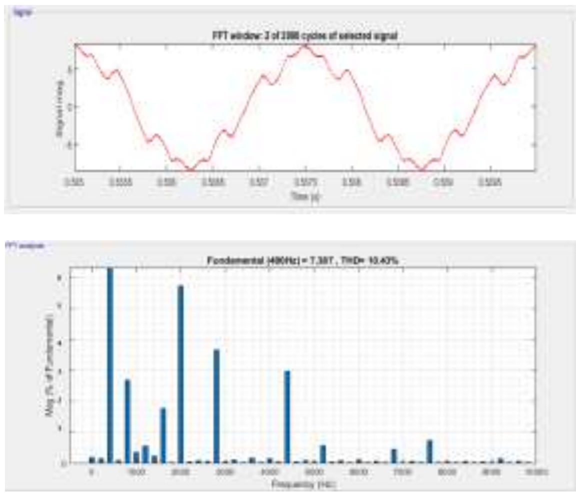


Fig 8: THD windows

From the THD window we can find that the distortion is significantly reduced to 10%. This is an important parameter to know about the possible losses. We this we can know how much distortion in just one cycle happens.

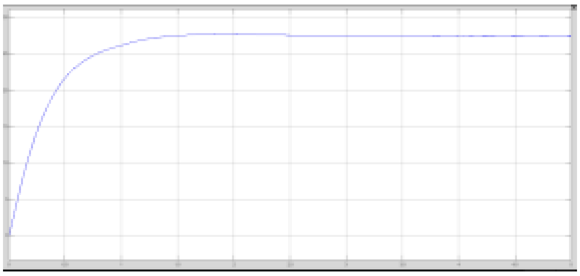


Fig 9 : Output waveform

From the output graph we can see that the high voltage is further reduced to a low voltage which is 28V. from a very high voltage of 415V the value has been decreased to this, making it more suitable for various uses.

11. CONCLUSION

In this comparison study we find that the modified version of the conventional structure is more efficient. Making it more efficient helps the system to be used in variety of places where low power voltage is required from a high voltage source.Lesser heat sinks make it more compact. Further the technique can be improved by using space vector modulation instead of pulse width modulation technique.

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