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"Comparison of Different Third Harmonic Injected PWM Strategies for 5-Level Diode Clamped Inverter"

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Abstract—In this paper, three modulation strategies based on a multicarrier level shifted PWM and third harmonic injected reference have been implemented; the aim of this paper is to compare these three strategies to know their effect on the output voltage quality of the inverter. The three modulation strategies are: Third Harmonic Injected reference In Phase Disposition (*THI-IPD*), Third Harmonic Injected reference Alternative Phase Opposition Disposition (*THI-APOD*) and Third Harmonic Injected reference Phase Opposition Disposition (*THI-POD*). These three strategies are applied to the single phase 2-legs 5-levels diode clamped inverter under different operation conditions. The study has been implemented via simulation using MATLAB/Simulink and setup experiments in the lab and the comparison between the simulation and experimental results are provided.

Keywords—5-level DC inverter, Third Harmonic Injected reference, level shifted PWM, THI-IPD, THI -POD and THI -APOD.

1. INTRODUCTION

Flying capacitor, Cascade and Diode clamped are the most popular multilevel inverter topologies. Numerous modulation strategies have already been reported to control the switches of these topologies. Of these modulation strategies, carrier-based modulations are considered the most common ones because of their inherent simplicity and their decreased computational requirements. Carrier-based modulation strategies are frequently established based on the carrier disposition technique for Diode-Clamped inverters, while they are extensively based on phase shifted technique for Cascade inverters. Each modulation strategy has its features which can be preferable or not preferable for a specific application [1]-[2]..

2. SINGLE PHASE 2-LEGS 5-LEVELS DC INVERTER

The topology that has been used in this paper is a single phase 2-legs five levels diode clamped inverter as shown in Fig. 1. With ***m*** being the number of output voltage level per leg (VAn, VBn), which is in this case equal to five. In general, the ***m*** level diode clamped inverter leg has ***(m-1)*** *dc* voltage inputs or *dc* link capacitor, ***2(m-1)*** switches per leg. The rating voltage of each switch is one *dc* voltage (*Vdc*) because when it is reversed it blocks a voltage level equals to *Vdc*. The required number of clamping diodes per leg *is* ***(m-1) (m -2)*** if the inverter is designed such that each clamping diode has the same voltage rating as the switches and the minimum diode reverse voltage is equal to *Vdc*. Otherwise, *2(m-2)* clamping diodes are required per leg with different ratings for reverse voltage blocking [3]. The output voltage for the Single Phase 2-legs 5-levels Diode Clamped Inverter per leg for each switching configuration is shown in table I.

It is clear from *table I* that there are not redundant switching configurations per leg for any *m*-level diode-clamped inverter leg; also, at any time there are *(m-1)* consecutive switches in *On* states, conducting. As the series of conducting switches moving from the top to the bottom end of the leg, the output voltage decreases from *2Vdc* to *-2Vdc* when the output is taken from *VAn* [3]-[4].

3. MODULATION STRATEGIES

In this paper, three modulation strategies have been conducted based on multi carrier level shifted PWM using third harmonic injected reference signal that obtained by adding the third harmonic sinusoidal signal with 1/6 of the peak of the fundamental to the fundamental sinusoidal signal to increase the fundamental component to 15% [5], as shown in Fig. 2. The three strategies have the same operation principle as follow:

The numbers of the needed carriers are (*m-1)* for *m*-level multilevel inverter, all carriers have identical frequency *fc* and peak-to-peak amplitude *Ac*. However, these carriers are shifted in levels to form adjacent bands. The numbers of the needed

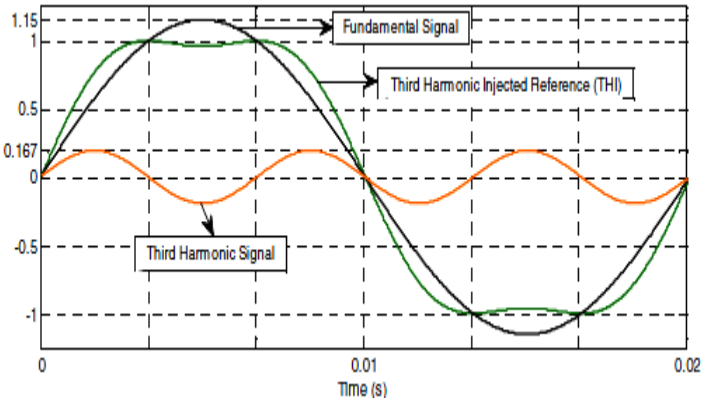

Fig. 2. Injection of third harmonic into sinusoidal signal.

4. MODULATION SCHEMES

In this section the different modulation schemes which are commonly prevailed for the control of DCMLI have been discussed. These modulation schemes are based on multicarrier based modulation which is further modified with third harmonic injection.

5. SINUSOIDAL PULSE WIDTH MODULATION (SPWM) WITH MULTI-CARRIER SCHEMES

In this section the control schemes for implementation of multi carrier modulation schemes with SPWM has been discussed. The following popularly implemented modulation schemes with a minor modification in the carrier wave form are shown below. The first scheme is the Phase disposition PWM Schemes with

Traingular Carrier (scheme 2)
With 3rd Harmonic Injection (scheme 1)

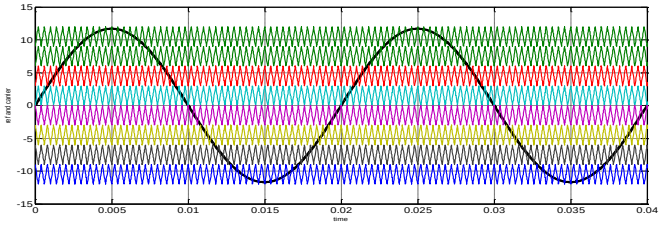

Figure 5.1 Carrier and reference wave form for scheme 2

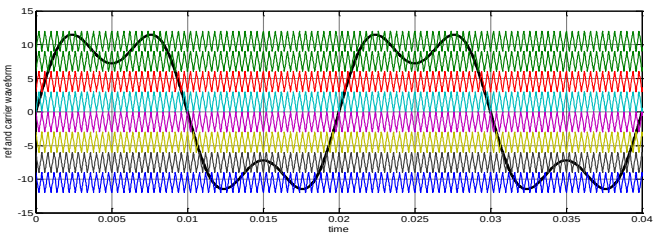

Figure 5.2 Carrier and reference wave form for scheme 1

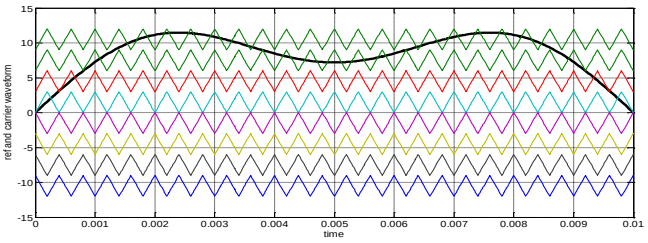

Figure 6.3 Carrier and reference wave form for scheme 1

6. VARIABLE AMPLITUDE PHASE DISPOSITION SCHEMES

Triangular Carrier (scheme 4)
With 3rd Harmonic Injection (scheme

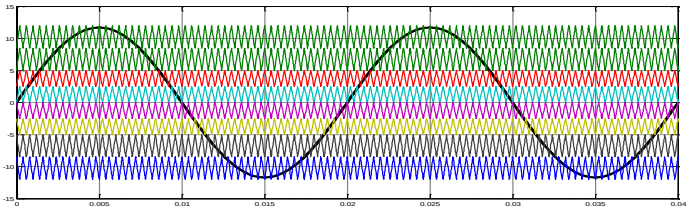

Figure 6.1 Carrier and reference wave form for scheme 4

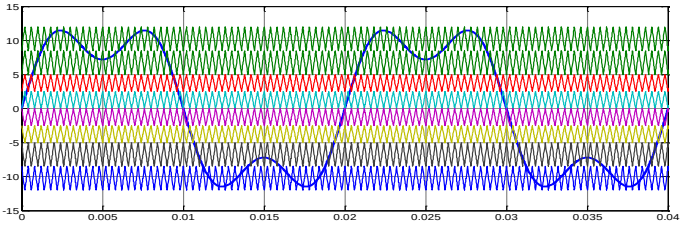

Figure 6.2 Carrier and reference wave form for scheme 3

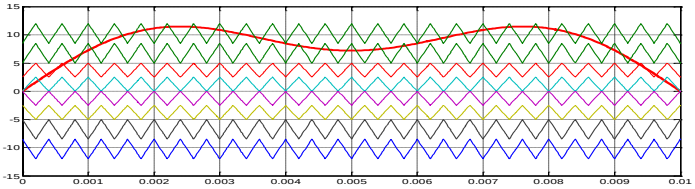

Figure 6.3 Enlarged Carrier and reference wave form for scheme 3

7. PHASE OPPOSITION DISPOSITION PWM SCHEMES

Triangular Carrier (scheme 6)
With 3rd Harmonic Injection (scheme 5)

As it can be seen from Fig.4.12 that in this modulation scheme sinusoidal multicarrier modulation with a reference sinusoidal waveform, with third harmonic wave is implemented. The alternate carrier waveforms are in phase opposition.

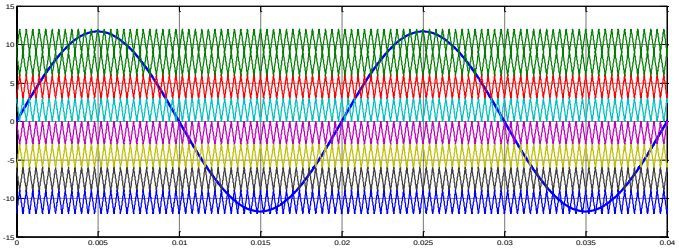

Figure 7.1 Carrier and reference wave form for scheme 6

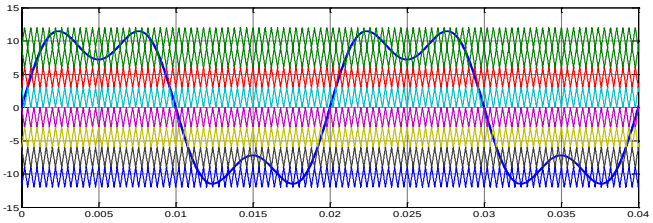

Figure 7.2 Carrier and reference wave form for scheme 5

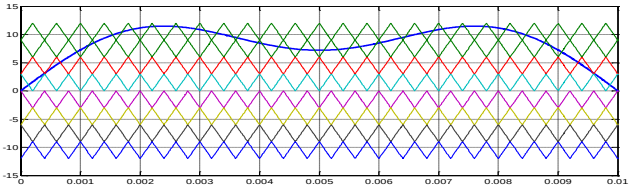

Figure 7.3 Enlarged Carrier and reference wave form for scheme 5

CONCLUSION

All the simulation model of diode clamped multilevel inverter is showing output waveform of minimum harmonics and improve power quality. The DCMLI inverter was studied by implementing the PWM and SPWM modulation techniques. The single phase three level and single phase five level Diode Clamped Multilevel inverters were simulated in MATLAB Simulink environment. The multicarrier modulations schemes line voltage and phase voltage modulation were implemented in these inverters. Diode Clamped Multilevel Inverters can achieve an effective increase in overall switching frequency through the cancellation of the lowest order switch frequency terms. This chapter has explained different types of carrier based PWM modulation techniques comes by different DCMLI models.PWM method are advantageous in controlling the output voltage and reducing the harmonics.

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