

Wireless Transmission of Data using LDPC Codes based on Raspberry Pi

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Abstract - This paper deals with the encoding and decoding of data using LDPC coding technique in a Raspberry Pi 3-B module. By utilizing two Raspberry Pi 3-B module, one for transmitter and another for receiver. Both the modules can be connected to each other using a same Wi-Fi network, by using the inbuilt WLAN 802.11b feature present in the module. The data is entered to the transmitter module (Tx) and it is encoded using LDPC coding technique, then encoded data is transmitted to the receiver module (Rx) by using the inbuilt WLAN 802.11b. After receiving the encoded data at the receive module (Rx), it is decoded using soft decision decoding or hard decision decoding, finally the original message is obtained. The bit-error rate is calculated and displayed on an LCD. LDPC coding technique is chosen since it has been proven to provide better performance than turbo codes or hamming codes or other coding techniques. LDPC codes have also been proven theoretically, it can reach the Shannon-Limit. Some of its major applications are IEEE standard 802.11, CMMB(China Multimedia Mobile Broadcast), DVB-S2(Digital Video Broadcast), 10 Gigabit Ethernet (10GBASE-T).

Key Words: LDPC, GUI, Shannon's limit, soft decision decoding, Raspberry Pi, Python.

1. INTRODUCTION

Wireless Communication is A mode of communication where huge amounts of data from one place or device to another place or device without the use of wires, cables and fibers. Wireless Communication could achieve high speed for data transmission (in Mbps, Gbps). But, during the transmission of data in channel, extra noise will be added, due to the noise, the data will be contaminated and performance will decrease. Hence, to avoid the noise, Channel coding techniques were introduced.

There are different types of channel coding techniques, for example Hamming codes, BHC codes, and LDPC codes. LDPC codes are linear block codes. It was introduced by Robert G Gallager, during his thesis for PhD. LDPC is known as Low Density Parity Check codes since it contain less number of 1s relative to that of 0s present in the **H** matrix, hence it is less complex in nature. The **H** matrix is defined as $[H] = [P^T I]$, where P^T is the transpose parity matrix. **H** matrix is constructed using Tanner graph. Using the **H** matrix we derive G matrix, which is multiplied by the input data. The G matrix is defined as $[G] = [P I]$. The encoded data is transmitted through the channel using

WLAN 802.11b. The transmitted data is decoded at the receiver using two types of decision decoding technique, soft decision decoding and hard decision decoding. Hard decision decoding is used for theoretical purpose and soft decision decoding is done for practical purpose, hence we use Sum-Product Algorithm (SPA) for decoding the received data.

$$H = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix}$$

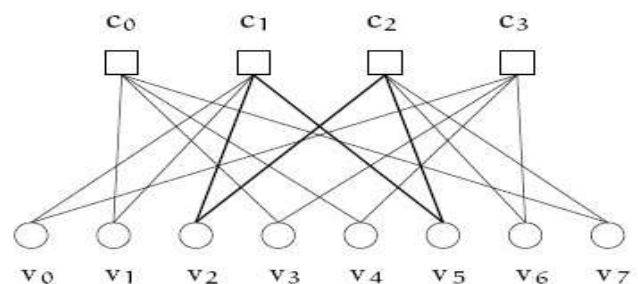


Fig-1: Standard H matrix and Tanner graph

The hardware is implemented based on Raspberry Pi 3-B module. It is used for transmission and receiving data. It has inbuilt WLAN 802.11b. It has a frequency of 1.2GHz and range of 50-100 m. It supports Raspbian software for programming, Python 3 is used as programming language.

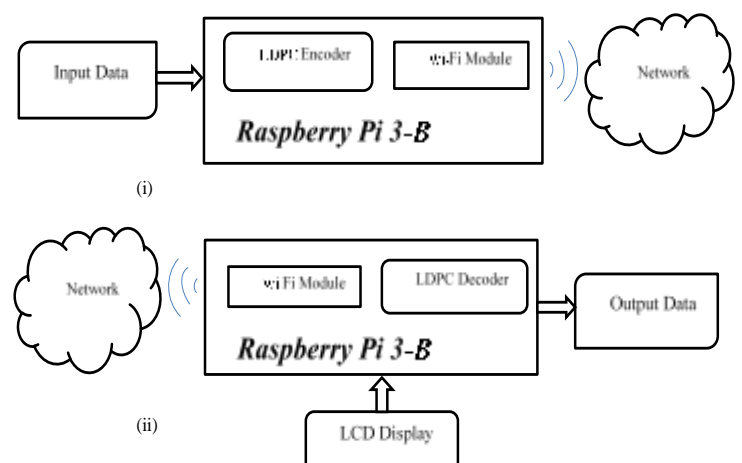


Fig-2: Transmitter (i) & Receiver (ii) Model Using Raspberry Pi 3-B

2. BACKGROUND/DOCUMENTARY RESEARCH

In the paper published by Swaraj Patil and Dr.D.P.Rathod has implemented the Raspberry Pi base wireless transmission of text data using LDPC codes. The encoding of the message data is done using lower triangular method. The LDPC parity matrix $[H]$ used here is regular, half code rate and size of the matrix is 8×16 . Sum-Product Algorithm is used to decode the data at the receiver. At the transmitter the text data is converted to ASCII format and then to binary for transmission. AWGN noise is added to the message data while transmitting. The hardware used here is Raspberry pi module one for receiver and another for transmitter. Both the modules are connected to the same server before the transmission of data. The encoding and decoding of the data is shown using GUI. [1]

In the paper presented by D.Chen, P.Chen and Yi Fang utilize encoding operation by a specific structure of LDPC parity matrix to parallelize row and column. An economical technique was additionally planned to regulate recollections, which may be reutilized for the LDPC code with completely different code rates to boost the economical utilization of hardware resources. The designed Low Density Parity Check encoder and decoder are simulated on Xilinx. According to simulation results of Model-Sim and MATLAB, they also verify that the proposed method has the advantages of reduced resource consumption, reduction in number of registers, low power and high accuracy. The proposed encoder can attain throughput up to 400 Mbps. Using this technique of encoding scheme they have shown that the decoding Bit Error Rate can be minimized at SNR less than 2.5 dB. [2]

A paper by Yuval.G, Olayinka.O, O.Oyerinde and Jaco Versfeld presents the development of a systematic quasi-cyclic (QC) LDPC code. This systematic structure is made by a row reduction technique totally different from the conventional mathematician elimination technique. The advantage of row reduction technique was being easier to implement when compared to mathematician row reduction technique. The projected row reduction technique maintains the similar cyclic structure and therefore the meagerness of the QC-LDPC redundant check matrix whereas providing a coffee quality approach to the development of the generator matrix. The projected construction exhibits associate economical BER performance for top rate codes, whereas being a less advanced encoder. [3]

In this paper M.Ushaswini Chowdary, B.Murali Krishna, K.S.N.Murthy, G.L.Madhumati, Habibulla Khan has worked on the ZigBee based wireless transmission of the data with LDPC codes using FPGA. Standard parity matrix is used of size 4×8 . Encoder is designed with generator matrix and decoder with Bit-flipping technique. The parity matrix is defined as $[H] = [A \mid I_{n-k}]$ and the generator matrix is obtained using the condition $G \cdot H^T = 0$. ISim tool of Xilinx is used to simulate the LDPC codes using Verilog HDL. The

hardware implementation of this project is done by dumping these codes on Spartan 3E FPGA board and verified the results. For low cost and low power design, they interfaced ZigBee module with FPGA. Since ZigBee module is used the data transmission range is short. For the hardware design only 3 Bit LDPC codes is considered for FPGA and ZigBee GPIO ports, and also can be implemented for high bit rates like 16, 32 bit and 64 bit.[4]

In the paper presented by Jayashree.C.N and Dr.Siddarama.R.P, their proposed work deals with design and implementation of flexible LDPC encoder using general and RU methods in ASIC FPGA. The versatile encoder designed with propagation delay of 208ns with $2/5$, $3/5$ rates of code. The design flexibility is capable of encoding at any rate and length of the parity check matrix. They analyzed the number of Slice LUTS, Number used as logic, Number of fully used LUT_FF, Number of Bonded IOB in ASIC FPGA. The propagation delay (propagation delay of 1.256ns) of encoder with RU method is minimum compared to general method. RU method encoding technique reduced complexity and improved speed. [5]

This paper proposes a low complexity LDPC design using message passing algorithm and systolic high throughput architecture. Whole LDPC design was designed simulated and synthesized using Xilinx ISE 13.1 EDA Tool. LDPC codes can attain the close to Shannon limit performance by iterative decoding process, here Threshold Controlled Min Sum Algorithm is used for decoding. They focus on the various levels of obstruction in decoding design. The decoder is designed and simulated using Xilinx ISE 13.1 and synthesized on Virtex-VI FPGA kits. [6]

In the paper published by R.Ramyashree, K.Bramaramba, Prof. A.Gopala Sharma, is based on LDPC coding system. The encoder is designed by standard encoding method and lower triangular modification. A random H (parity check) matrix is derived from the tanner graph based on the size of the data which has to be transmitted. From the H matrix, generator matrix (G) is derived. The message is then encoded and transmitted through AWGN channel. Novel BP algorithm is used for decoding the received data at the receiver end. Two Raspberry Pi module is used one at transmitter end and another at the receiver end. They sent data from encoder through AWGN channel and received the encoded data in decoder, where the data is decoded and the original message is retrieved. They hope to implement this technique for mobile GPU, while CPU performs other tasks in parallel. [7]

Nelson Alves Ferreira Neto, Joaquim Ranyere S. First State Oliveira, Wagner Luiz A, First State Oliveira and Joao Ilich Sanchez N. Bittencourt given 2 architectures for the density verification (LDPC) encoder, the primary one supported a totally serial approach and therefore the other in a very mixed method, likewise as their corresponding realizations in ASIC. The planned styles are able to operate in eighty four combos of code rate and word size, in line with the IEEE

802.22 Wireless Regional space Network (WRAN) customary, aiming low power and economical utilization of space. Though the planned architectures are primarily designed for the mentioned customary, they will be simply changed to different wireless broadband standards. The planned architectures were established effective in meeting the necessities of knowledge rate demanded by the 802.22 customary. It absolutely was attainable to form LDPC encoders compatible with eighty four completely different configurations, intense smaller space and power inherent within the sort of application. [8]

In this paper we observe, the decoders are designed based on the LDPC convolutional codes (LDPCCC). These decoders uses GPU parallel architecture. Decoders use thread layout and data structure, also they minimize the thread divergence, which leads to the access of memory in combined way. They have designed the decoders to be flexible and scalable, like the decoder works on 32 codes, but they can be used even for 64 codes. The results prove that GPU parallel architecture produces better results than parallel solutions from VLSI or FPGA. When the results are compared with the traditional CPU-based decoders, the GPU-based decoders produce 100x to 200x speed. [9]

In this paper they proposed a novel triple-concatenated forward error correction for 100 GB/s transmission. Simulation shows that a net coding gain of 10.8dB is obtained by a soft-decision LPDC code concatenated with the enhanced FEC listed in G.975.1.[10]

This paper describes a senior-level undergraduate class project that simulates a communication system using LDPC as the error correction code. Usually, LDPC codes are introduced in coding theory, error correction code, or information theory classes at graduate level. However, the LDPC code itself as a particular example of error correction code can be explained without using advanced mathematics because it can be understood by basic factor graphs and simple linear algebraic operations. Hence, a LDPC error correction simulation is a good sample project that intrigue students and entices them to further the study of coding theory. The class project was successfully implemented based on a GUI environment, and it correctly allows the student to understand the usefulness of error correcting codes within a larger communication system. The successful completion of the project proves that a simple introduction of LDPC codes with graphs and basic linear algebra is enough for undergraduate students to realize the functionality of error correction coding techniques in communication systems. Moreover, students suggested that more projects along the lines of the one hereby presented should be included throughout the curriculum. [11]

In this paper the authors proposed some reduced complexity decoding strategies to decrease the storage requirements and initial decoding delay without any loss in data or information. At the transmitter end, partial syndrome

encoder is used for encoding the data because of its high efficient transmission of streaming data, since they allow continuous encoding and decoding. The partial syndrome former encoder is implemented using a shift register. In the decoder part, they terminate the encoder sequence to form a frame of pre-determined length. The received data is then decoded using message-passing algorithm. In this paper, they compare several aspects of decoding a message LDPC convolution codes to LDPC block codes, also they studied the dependence of the BER and SNR for terminated codes. [12]

In the paper published by B. Djordjevic, M. Cvijetic, L. Xu, and T. Wang. They projected a coded modulation schemes for ultrahigh-speed transmission (100 GB/s and above). The modulation was done on the premise of construction modulation and coherent detection was found to perform the direct detection one and to supply extra margin for extended transmission of information. Mistreatment this method coherent detection theme may be effectively accustomed extend the info transmission distance by concerning 25%, and this was left for future analysis. [13]

3. RESOURCES FOR HARDWARE & SOFTWARE

- Raspberry Pi 3 Model B+ microcontroller
- SD card (16GB)
- USB cable



Fig-3: Raspberry Pi 3 Model B

- Raspbian
- Python 3 (programming language)



Fig-4: Raspbian with Python coding

4. CONCLUSION

In this paper we analyze papers and projects worked on LDPC. By the analysis, we conclude that LDPC codes perform better than other FEC (forward error correcting) techniques and it is theoretically proven that LDPC codes reach Shannon limit. LDPC codes can be used with the help of flexible architecture, which utilizes less power and at low cost. The decoder design is also less complex.

5. FUTURE SCOPE

LDPC codes beat turbo codes to become error correcting code in the new DVB-S2 standard. LDPC codes beat convolution turbo codes as the FEC system for the ITU-TG.hn standard. LDPC codes are also used for 10G Base-T Ethernet, it sends data at 10gbps. LDPC codes are also part of Wi-Fi 802.11 standard. LDPC codes are being implemented in 5G communication system.

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