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MICROFABRICATION PROCESS & EQUIPMENTS

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Abstract - *Microfabrication is the process of fabricating small structure usually in micrometer scale. Micro fabrication was initially developed from microelectronics industry, and the devices which are usually made by silicon wafers even though glass, plastics and many other substrates are in use. Silicon is the main semiconducting device used in the fabrication of microelectronic. Substrate is the back bone of micro fabrication upon which entire system is built up. For electronic applications, semiconducting substrates such as silicon wafers can be used. The basic micro fabrication process consist of Patten generation, optical lithography, etching, wafer cleaning and surface preparation, Thermal oxidation, diffusion, Ion Implantation, Chemical Mechanical polishing, bonding and layer transfer, Moulding and stamping. The micro fabrication process involves Physical, chemical conditions of each process are carry out in different tool condition. Silicon wafer manufacturing is a multistep process which begins with purification of sand and ends with polishing and defect inspection. The tool sizes of micro fabrication are inversely proportional size of structure.*

***Key Words*: Microfabrication Process & Tools - Silicon Crystal Growth - Wafer processing - Optical Lithography - Etching,**

1. INTRODUCTION

Microfabrication is the process of fabricating small structure usually in micrometer scale. Micro fabrication is process of a collection of technologies which are used for making micro devices Its main application include in manufacturing process of MEMS (micro electro mechanical system), integrated circuit, micro optics, solar cell etc. Micro fabrication process earlier used in the manufacturing of integrated circuit was known as semiconductor manufacturing [1]. Micro fabrication technologies started from the microelectronics industry, and the devices which are usually made by silicon wafers even though glass, plastics and many other substrates are in use

Silicon is the main semiconducting device used in the fabrication of microelectronic. This is because due to the advantage of silicon by varying its resistivity by eight order of magnitude which results many micro structure during doping. Silicon microelectronic devices possess higher complexity and miniaturization [2]. Silicon optoelectronic devices are used in light detectors. Other desirable property of silicon is its extremely strong structure and low cost for single crystal wafer and also it is one of the common elements available on the earth. They possess varying electrical property according to varying voltage applied on it. Pressure sensors, resonators, gyroscopes, switches and other mechanical and electromechanical devices utilize the excellent mechanical properties of silicon. Hence silicon is considered as precise platform for the manufacturing of many electro devices. Resistivity of silicon wafer ranges from .001 – 20000 ohm-cm.

Substrate is the back bone of micro fabrication upon which entire system is built up. For electronic applications, semiconducting substrates such as silicon wafers can be used[3]. For optical devices or flat panel displays, transparent substrates such as glass or quartz are common. The substrate enables easy handling of the micro device through the many fabrication steps .various individual devices are built upon a single substrate and then form into separated devices toward the end of fabrication.

The basic microfabrication process consist of Patten generation, optical lithography, etching, wafer cleaning and surface preparation, Thermal oxidation, diffusion, Ion implantation, Chemical Mechanical polishing, bonding and layer transfer, Molding and stamping[4].

Thin film steps are used to make structures metallic dielectric and semiconducting film. Wafer bonding and layer transfer enable more complex structure to be made. Micro fabrication takes place under carefully controlled conditions of particle purity, temperature, humidity, and vibration because otherwise micrometer scale structure would be destroyed. The wafers are cleaned actively during processing with enough demonized water. Micro fabrication involve various Physical chemical condition, each process are carry out in different tool condition.

2. MICROFABRICATION PROCESS AND TOOLS

The microfabrication process involves Physical chemical condition each process are carry out in different tool condition. Silicon wafer manufacturing is a multistep process which begins with purification of sand and ends with polishing and defect inspection. The tool sizes of micro fabrication are inversely proportional size of structure. Microfabrication takes place under highly controlled conditions that is all materials for clean room construction, processing equipment and wafer-handling tools are carefully selected to minimize particle, molecular or ionic contamination. Water, gases and chemicals are purified from contaminants and filtered of the particles. These are, however passive precautions and active wafer cleaning must be undertaken before the practically every major process step. Wafer-cleaning steps can account for up to 30% of all process steps.

Wafer cleaning is a process of contamination control, but also it leaves the surface in a known and controlled condition. This means damage removal, surface termination (hydrophobicity/ hydrophilicity control) and prevention of unwanted adsorption. Therefore, many people prefer to call this activity as surface preparation. The main sources of contamination are the fabrication processes by themselves. Air cleanliness is conducted in an advanced clean room is so good because airborne particles are not the main contamination source anymore, but airborne gaseous contaminants need careful attention. The human contribution has also been reduced significantly with correct gowning and working procedures or by factory automation.

2.1 Cleanliness

Microfabrication process takes place under carefully controlled conditions, such as particle purity, temperature, humidity and vibration .Otherwise micrometer scale structures would be destroyed by particles or else lithography process would be ruined by vibrations or temperature and humidity fluctuations. Clean room designs are shown in Figure .High-efficiency filters can be placed locally or they can have 100% coverage, offering improved cleanliness and laminar (unidirectional) airflow. Wafers are cleaned actively during this processing; hundreds of liters of ultrapure water (de-ionized water, DIW) are used for each wafer during its fabrication. This is the dynamic part of particle cleanliness. The passive part comes from careful selection of materials for clean room walls, floors and ceilings, including sealants and paints, plus process equipment, wafer storage boxes and all associated tools, fixtures and jigs.

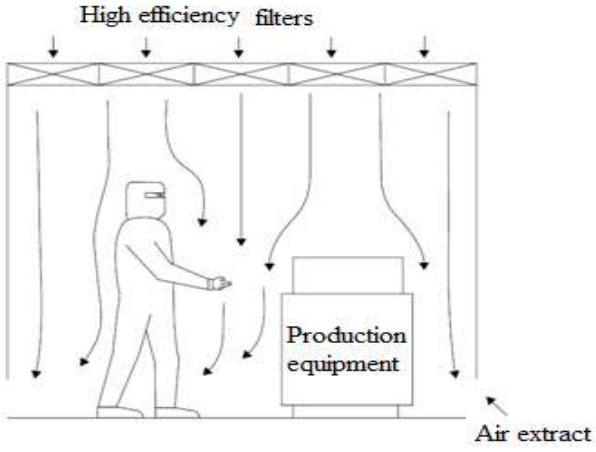


Fig. 2.1 Clean room

3. SILICON CRYSTAL GROWTH

In this process (Czochralski crystal growth) the silica crucible (SiO2) is filled with undoped electronic grade polysilicon. The dopant is introduced by adding pieces of doped silicon (for low doping concentration) or elemental dopants P, B, Sb or As (for high doping concentration). The crucible is heated in vacuum to 1420 ◦C to melt the silicon which is shown in figure. A single crystalline seed of known crystal orientation is dipped into the silicon melt[3]. The silicon solidifies into a crystal structure determined by the seed crystal. A thin neck is quickly drawn to suppress the defects that develop because of a large temperature difference between the seed and the melt, and then the pulling rate is lowered. Both the ingot and the crucible are rotated (in opposite directions).The ingot rotation is 20 rpm and crucible rotation about 10 rpm. The diameter of ingot is determined by the pull rate of ingot and the length of ingot is related to the size of crucible.

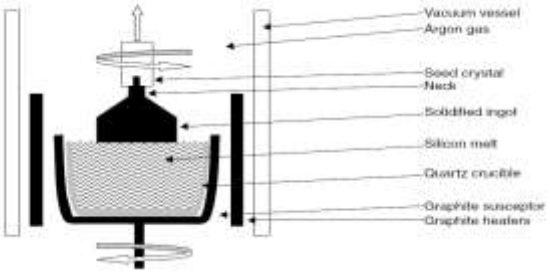


Fig. 3.1 Czochralski crystal growth

3.1 Silicon wafer slicing

- Ingot crystal orientaion by XRD
- Flat grinding
- Sawing ingot into wafers
- Lapping
- Edge smoothing
- Laser scribing
- Etching
- Annealing to destroy thermal donors
- Final polishing
- Inspection

Above are the lists of tools used to transform the ingot into wafer. The ingots are cut in to 50cm stock X-ray test is conducted for determining the crystal orientation. A flat or notch are then ground in to the ingot to establish the wafer orientation and type of doping. The next step is lapping. The waviness and taper from the sawing are removed by lapping. In lapping, the wafers are rotating between two massive steel plates with alumina slurry. Surface roughness is 0.1 to 0.3μm after the lapping step[4]. The edges of the wafers are then beveled in order to prevent the chipping of silicon during wafer handling. Etching is then used to remove the lapping damage both alkaline (KOH) and acidic (HF-HNO3) etches can be used. Roughness is reduced in acid etching. An annealing step at 600 to 800 ◦C destroys thermal donors that are charged interstitial oxygen complexes. Final polishing with 10 nm silica slurry is used for removing alkaline

solution and results in 0.1 to 0.2 nm RMS surface roughness. Silicon is lost in the above-mentioned steps and the half of the original ingot ends up as wafer material.

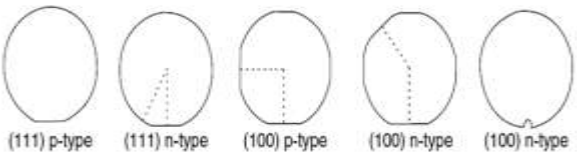


Fig. 3.2 Wafer orientation and doping type

4. WAFER PROCESSING

Wafer processing is initial step in micro fabrication it can be done either in batch processing or in single wafer processing. In earlier microfabrication, cost minimization were resulted from the batch processing because of many wafers are handled simoultanousily in a furnace, wet etch bench.

But now days in order to obtain more scale down line width increase in the demand of process control and hence single wafer tools have suppressed batch equipment's.

In batch process a cassette of wafers are processed simultaneously in wafer cleaning and non pattern etching which removes excess oxide by hydrogen fluoride, which are commonly done in batch processing. But when line widths are below 3µm batch wet processing is very difficult due to high process control. Batch processing results in the uniformity among the wafer processed.

In single wafer processing due to robotic loading and unloading factory automation is much easier. Thin films require less process time than thick film which favors single wafer processing [4]. In single wafer processing wafer to wafer repeatability is major issue. Another main advantage of Single-wafer processing is the, easy process development because fewer wafers are needed and batch effects are eliminated. In epitaxy, single-wafer and batch tools co-exist, but in plasma etching and sputtering, single-wafer tools are the norm in mainstream IC production.

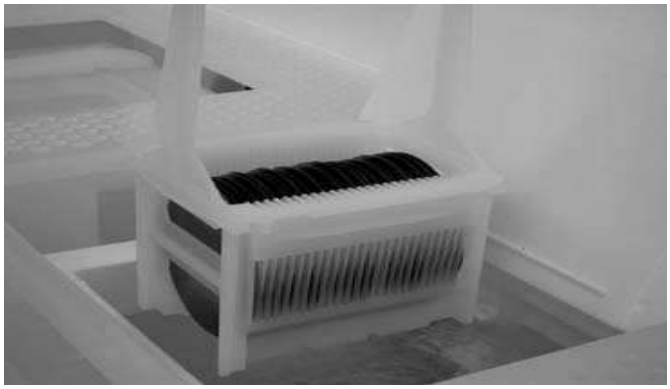


Fig. 4.1 Cassettes of wafers

4.1 Deposition and growth

Micro fabricated devices are typically constructed using one or more thin films .The purpose of these thin films depends on the type of device. Electronic devices may have thin films which are conductors (metals), insulators (dielectrics) or semiconductors. Optical devices may have films which are reflective, transparent, light guiding or scattering. Films may also have a chemical or mechanical purpose as well as for MEMS applications. Silicon dioxide has a function of capacitor die electric and isolation material. Silicon dioxide act as a masking material during silicon processing such as diffusion and etching .One of the important thin film deposition is chemically vapour deposition. The reacter consists of a tube with a heated susceptor on which the wafer rest an inlet and outlet permit flow of the gasses over the surface of the wafer.

$SiH_{4\,(g)} + O_{2(g)} - (h) \rightarrow SiO_{2(s)} + 2H_{2(g)}$

In this reaction, silane (SiH_4) and molecular oxygen enter the reactor at outlet, under proper condition reaction take place on wafer at 425°C.

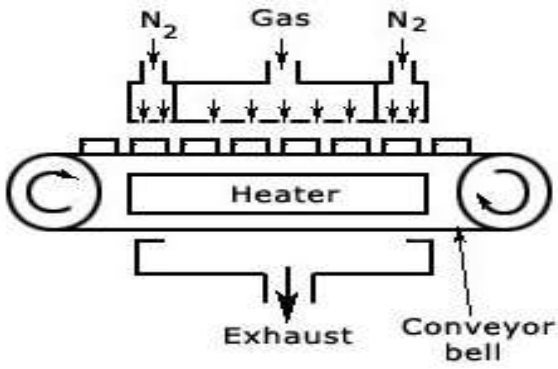


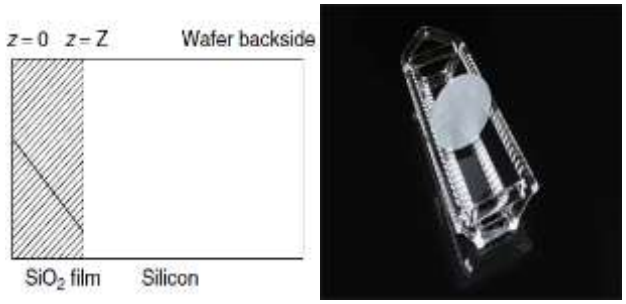
Fig. 4.2 Chemical vapor depositions with conveyor

4.2 Thermal oxidation

The technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it. Silicon is easily oxidized. A native oxide of nanometer thickness grows on the silicon surface in a couple of hours or days, depending on surface conditions, and similar thin oxides form easily in oxygen plasma or in oxidizing wet treatment. These oxides are, however, limited in their thickness and they are not stoichiometric SiO2. Deposited CVD oxides are used in some applications where low temperatures are absolutely necessary, but superior silicon dioxides are grown in 800 to 1200 ◦C. Thermal oxidation can be classified into wet oxidation and dry oxidation

Wet oxidation: Si (s) + 2H2O (g) −→SiO2 (s) + 2H2 (g)

Dry oxidation: Si (s) + O2 (g) −→ SiO2 (s)



Heat wafer in an atmosphere $Si + O_2 \rightarrow SiO_2$

Containing an oxidant, usually O_2 $Si + 2H_2O \rightarrow SiO_2 + 2H_2$

steam or N_2O $Si + 2N_2O \rightarrow SiO_2 + 2N_2$

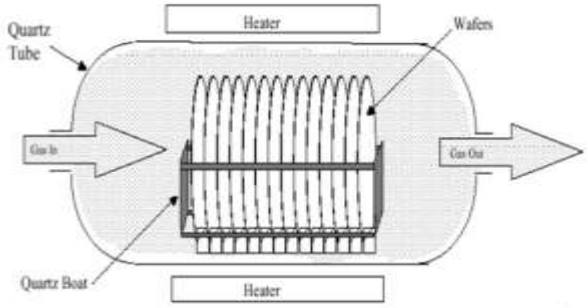


Fig. 4.3 Thermal Oxidation furnace & Quartz rack Boat

Thermal oxidation is a slow process. Dry oxidation takes place at 900 ◦C for 1 hr produces 20 nm thick oxide and wet oxidation for 1 hr produces 170 nm. Exact values are dependent on silicon crystal orientation. Most thermal oxidation is performed in furnaces, at temperatures between 800 and 1200 °C. A single furnace accepts many wafers at the same time, in a specially designed quartz rack (boat). When the boat enters the oxidation chamber from the side, the design is called horizontal, and kept the wafers vertically, beside each other. But many modern designs hold the wafers horizontally above and below each other and load them into the oxidation chamber from below [7]. Vertical furnaces stand higher than horizontal furnaces, so they may not fit into some microfabrication facilities and also they help to prevent dust contamination. Unlike horizontal furnaces, in which falling dust can contaminate any wafer. But vertical furnaces only allow it to fall on the top of the wafer in the boat. Horizontal furnaces typically have convection currents inside the tube which causes the bottom of the tube to be slightly colder than the top of the tube. As the wafers lays vertically in the tube the convection and the temperature gradient causes the top of the wafer to have a thicker oxide layer than the bottom of the wafer. Vertical furnaces solve this problem by having wafer sitting horizontally and then having the gas flow in the furnace flowing from top to bottom.

4.3 Patterning

It is the process of obtaining the desirable features in to a film. The pattern defines the photomask for removing the portion of material. The simplest photomask consists of laser printed over the transparencies. They are suitable for structures in the size range from hundreds of micrometers. Photomasks consist of glass plates with chromium (100nm thick).Soda lime glass is used for larger line width (>3μm) .The three basic important points of photomasks are line width, position and defects. Line width is the local measurement, over a test structure pattern.

4.4 Beam writing

Electron and laser beam are the standard tool for pattern generation. The simplest writing strategy is termed raster scan. It uses a single Gaussian beam and divides the pattern to be drawn into small rectangles and makes an 'exposure-no-exposure' decision for each rectangle. Vector scanning enables skipping of empty (non-exposed) spaces, making the system much faster, at the expense of system complexity. Variable shaped beam is another improvement over raster scan. When larger than the minimum pixel size structures are to be drawn then writing speed is enhanced. Electron beam and laser beam writing area is very small: 250 × 250μm area, that is, the area that can be scanned electromagnetically. Beam spot can be even obtain at range of 5nm.

4.5 Defect in photo mask

Defect on the mask are classified two board categories such as hard defect and soft defect. Soft defect are mainly particles or resist residue that can be cleaned away. Hard defect are permanent spots or scratches. In case of repair point of view two classes of defects are missing chrome and extra chrome. The missing chrome requires deposition of layer that will prevent light transmission. The extra chrome requires removal chrome. Defect on mask are significant as they will reproduced on the wafer .some of the common defect are

- Protrusion -extra chrome attached to a feature
- Intrusion -partial loss of chrome in a feature
- Bridge -chrome connecting two features
- Necking -discontinuity in a line
- Pinhole-hole in chrome
- pin spot -extra chrome on a light field area.

Fig. 4.4 Defect in photo mask

5. OPTICAL LITHOGRAPHY

Lithography work flow consists of the following major

Steps when viewed from the point of view of the wafer:

1. Photosensitive film (photoresist) application
2. Alignment of mask and wafer
3. Exposure of the photoresist
4. Development of patterns.

Optical lithography is basically photography. The original image which is to be transferred to the photomask, form a the negative image in photography. This is set in a mask-aligner/exposure tool. Then it is aligned to the photoresist-coated wafer, and exposed by UV radiation. Exposure changes photoresist solubility, which enables selective removal of resist in the development step. Photo resist are classified into positive resist and negative resist. In positive resists, the exposed areas become more soluble in the developer, and in negative resists, the exposed parts become insoluble.

5.1 Photoresist application

The wafer is covered with photoresist by spin coating. A viscous, liquid solution of photoresist is dispensed onto the wafer, and the wafer is spin rapidly to produce a uniformly thick layer. The spin coating typically runs at 1200 to 4800 rpm for 30 to 60 seconds, and produces a layer between 0.5 and 2.5 micrometers thick. The spin coating process results in a uniform thin layer, usually with uniformity of within 5 to 10 nanometers. This uniformity can be explained by detailed fluid-mechanical modeling, which shows that the resist moves much faster at the top of the layer than at the bottom, where viscous forces bind the resist to the wafer surface. Thus, the top layer of resist is quickly ejected from the wafer's edge while the bottom layer still creeps slowly radially along the wafer. In this way, any 'bump' or 'ridge' of resist is removed, leaving a very flat layer. Final thickness is also determined by the evaporation of liquid solvents from the resist. The photo resist-coated wafer is then prebaked to drive off excess photoresist solvent, typically at 90 to 100 °C for 30 to 60 seconds on a hotplate.

5.2 Spin coating

It is a procedure used to deposit uniform thin films to flat substrates. Usually a small amount of coating material is applied on the center of the substrate, which is either spinning at low speed or not spinning at all. The substrate is then rotated at high speed in order to spread the coating material by centrifugal force. A machine used for spin coating is called a spin coater, or simply spinner. Rotation is continued while the fluid spins off the edges of the substrate, until the desired thickness of the film is achieved. Depending on the wafer size and desired film thickness, a drop of 1 to 10ml is dispensed at the wafer center. Acceleration to 5000 rpm spreads the liquid towards the edges. Half of the solvent can evaporate during the first few seconds, so rapid acceleration is a must because viscosity changes with solvent content, and radially non-uniform thickness will result from viscosity differences. Spin speed can be controlled to ±1 rpm, and an error of ±50 rpm will result in 10% thickness differences. So, the higher the angular speed of spinning, the thinner the film. The thickness of the film also depends on the viscosity and concentration of the solution and the solvent. A widely studied phenomenon in spin-coating is the coffee ring effect.

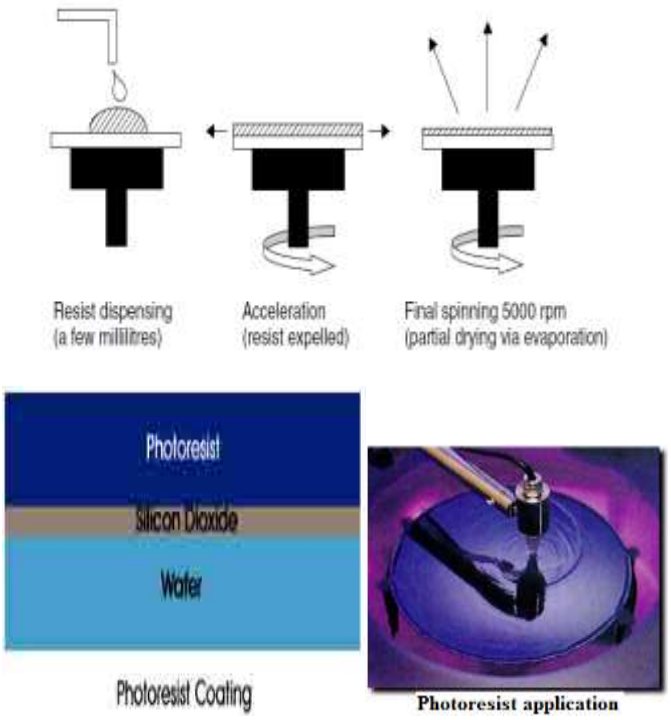


Fig. 5.1 Spin coating

5.3 Allignment of mask

The simplest lithographic technique is contact lithography. The photo mask and the resist-covered wafer are brought into intimate contact, and exposed. The

resolution is determined by mask dimensions and diffraction at mask edges. Extremely small patterns can be made in theory but making photo masks with submicron features is prohibitively expensive. Damage to the mask is frequent when the mask and the wafer are brought into contact, which makes contact printing not very production worthy. Proximity lithography is a modification of contact lithography. A small gap, for example, 3 to 50μm is left between the mask and the wafer. The wave front traversing the mask is diffracted by the mask patterns, and Fresnel diffraction formulae have to be used to estimate resolution. Both contact and proximity lithography is done in one and the same machine, the gap between the mask and the wafer is an adjustable parameter. The image is the same size as the original. The role of optical system 1 is then to provide uniform illumination. Optical system II does not exist. In projection optical systems, the optical system II is the key element. It provides an image of the mask on the wafer. Reduction optics can be used, and this is a great improvement With 5X reduction projection optics, the original photo mask features can be made rather large.

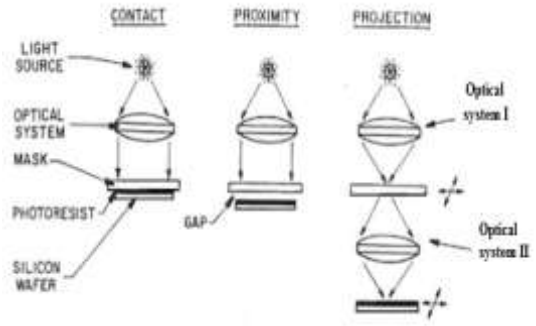


Fig. 5.2 Optical lithography

5.4 Exposure and developing

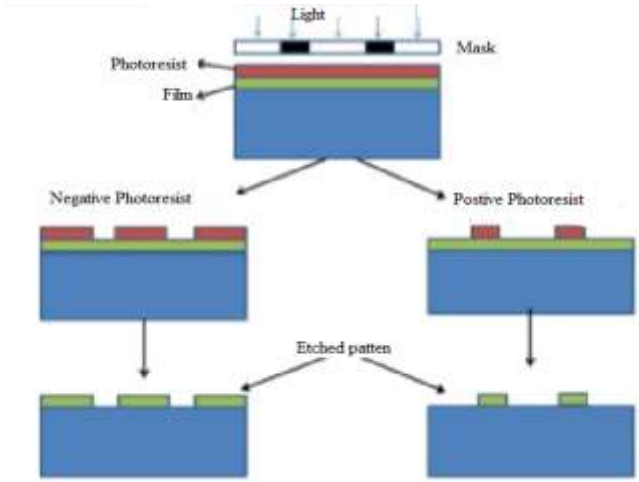


Fig. 5.3 Positive and negative photo resist

After prebaking, the photoresist is exposed to a pattern of intense light. The exposure to light causes a chemical change that allows some of the photoresist to be removed by a special solution, called "developer". Positive photoresist, the most common type, becomes soluble in the developer when exposed; with negative photoresist, unexposed regions are soluble in the developer [6].

6. ETCHING

Etching is the removal of some portion of the thin film or substrate. The etching process consist of three steps

1) Transport of etchants to surface.
2) Surface reaction.
3) Removal of product.
4) The etching processes are classified in to two types' wet etching and plasma etching.

6.1 Wet etching

Solid + liquid etchant=soluble product

The wet etching processes used liquid-phase etchants. The wafer can be immersed in a bath of etchant, which must be agitated to achieve good process control. For instance, buffer hydrofluoric acid (BHF) is used commonly to etch silicon dioxide over a silicon substrate.

Wet etchants are usually isotropic, which leads to large removal when etching thick films. They also require the disposal of large amounts of toxic waste. For these reasons, they are seldom used in state-of-the-art processes.

Wet etching tools are comes in three major variants: tank (bath), spray tool and single-wafer processor. The tank is a quartz vessel with heating and temperature control. It is filled with water and chemicals and the wafers are immersed in liquid for the required time, and then transferred to similar tanks for rinsing. Spray tools handle a cassette but instead of immersion, liquid is sprayed from stationary nozzles on rotating wafer cassette. After the first spraying, the process continues with either another chemical or DI-water spray and nitrogen is used for drying in the same vessel. Fresh mixing of chemicals and lower liquid volumes of spray are the advantages. Single-wafer tools are same as to the photo resist spinners, and in a sense, they are spray tools. However, processing acts on the wafer topside only. The heating of wet process tanks uniformly is not a easy task, because highly reactive and corrosive chemicals are used at high temperatures (e.g., 180 ◦C boiling nitric acid to etch nitride, or 120˚C peroxisulphuric acid for cleaning, known as Piranha). The materials of the tanks and heaters must be compatible with the process in chemical, thermal and mechanical aspects.

Teflon_ and quartz are often used in the most demanding applications, but both are expensive materials and difficult to machine. Polypropylene is used for less critical applications, while stainless steel is the material for solvent tanks.

6.2 Plasma etching

Solid + gaseous etchant = volatile product

Plasma etching is used to fabricate integrated circuits. It involves a high-speed stream of glow discharge (plasma) of an appropriate gas mixture being shot (in pulses) to a sample. The plasma source is known as etch species which can be either charged (ions) or neutral (atoms and radicals). During the process, the plasma will generate volatile etch products at room temperature by the chemical reactions between the elements of the material etched and the reactive species generated by the plasma. The atoms of the shot element embed themselves at or just below the surface of the target, thus modifying the physical properties of the target. Plasma etching process depends upon.

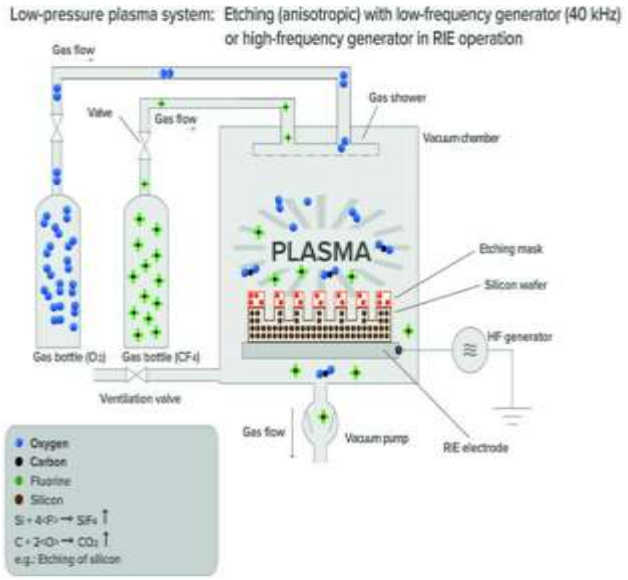


Fig. 6.1 Plasma Etching

- The Electron source
- Pressure
- Gas species
- Vacuum

6.3 Diffusion

It is the process of introducing n-type or p-type into silicon. The power of silicon is mainly depends upon the concentration of dopant. Dopant can implemented in to silicon in many ways during crystal growth, during epitaxy, by ion implementation etc. Usually diffusion are conducted at temperature of 900-1200^{0}C .Diffusion is the movement of atom along the concentration gradient which are classified in to three ways named as interstitial, substitutional, interstitilacy. In interstitial diffusion atoms jump from one interstitial site to another, which is always available. The substitutional diffusion indicates that empty lattice place is available next to the diffusion atom. The interstitiliacy diffusion is related to substitutional diffusion. The self-interstitial atoms move to the lattice sites, and kick the dopants to the interstitial sites, and from there they move to the lattice sites.

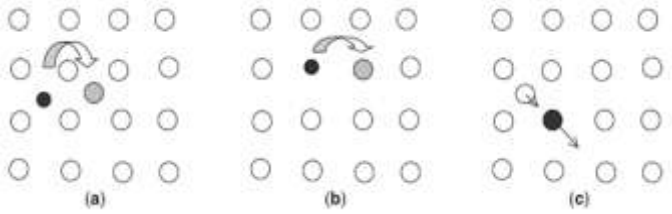


Fig. 6.2 Diffusion
(a)interstitial(b)substitutional/vacancy(c)interstitial

Measurement of diffusion profile can be read by physically or electrically. The physical measurement is known as secondary ion mass spectrometry (SIMS). dopant concentrations of 10^{14} to 10^{16}/cm^3 can be detected (silicon atom density is 5×10^{22}/cm3).The electrical measurement is known as spreading resistance (SRP) measurement ,which measures resistance with probes at the surface, and then beveling or anodic oxidation is done in order to have access to the dopants deeper inside the silicon. SRP data needs some heavy calculations before dopant profiles are obtained. Both SIMS and SRP are sample destructive methods.

6.4 Ion Implantation

It is the process of accelerating Ion in to the silicon wafer, which hit, and penetrate into the silicon, slowly by collisional and stochastic processes and come to rest within few seconds at the top micrometer layer. Ion implantation can be used to produce a great variety of doping profiles inside silicon. Maximum dopant density not be in the wafer surface; it is in the hundreds of nanometers deep inside the silicon. Iron implantation uses voltage range of 20kv-200kv.iron implantation are classified in to three types High energy implanter, Low energy implanter & Medium energy implanter. High current implanter uses 2MeV; low energy implanter uses 1keV & Medium energy 20ke-200keV.Low energy implanter, implant 100nm, High energy implanter, implant 1micro meter. Medium implanter uses single wafer machine. High implanter uses batch machine. Normal case, implant current varies from 1μA to 30mA. Iron implantation requires iron sources (plasma sources).The dopant has to be gaseous before ionization. The dopant gases are PH_3, AsH_3,BF_3.

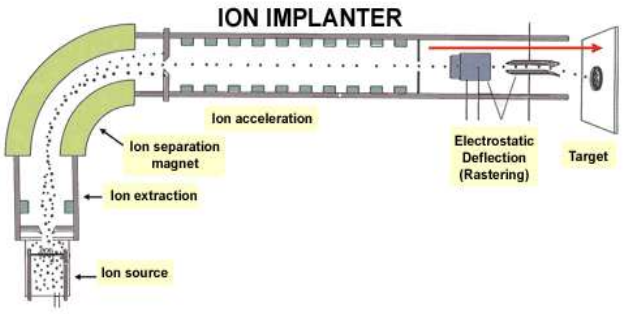


Fig. 6.3 Ion implanter

The ions are extracted from the source which is extracted by voltage, which is entering in to the selection magnet. Ion selection is based on mass spectrometric separation according to the radius of curvature. By adjusting the magnetic field the selection of ion of desired mass is selected. The acceleration tube must be kept in high vacuum in order to control the beam collision less fashion. After acceleration, either electromagnetic or mechanical scanning spreads the beam over the wafer. Implantation is a slow process because of the scanning nature of the operation. The wafer will charged when ions are implanted. The current flows from the beam to the wafer holder, and it passes any oxides on its way. Also, beam non uniformity between the wafer centre and the edge can cause lateral currents. Implantation is monitored by Fraday cup current measurement.

6.5 Chemical mechanical polishing

In Chemical mechanical polishing removes very small amount of micrometers only which results surfaces are very smooth and defect free. The CMP tool consists of a solid, which is extremely flat platen, on which the polishing pad is glued. The wafer chuck, which holds the wafer upside down, which is situated on a spindle [9]. A slurry introduction mechanism feeds the slurry on the pad. Both the platen and the spindle are rotated, and the linear velocity is the sum of two velocities.

There are four major elements in a CMP process:

• Topography

• Materials

• polishing pad

• Slurry.

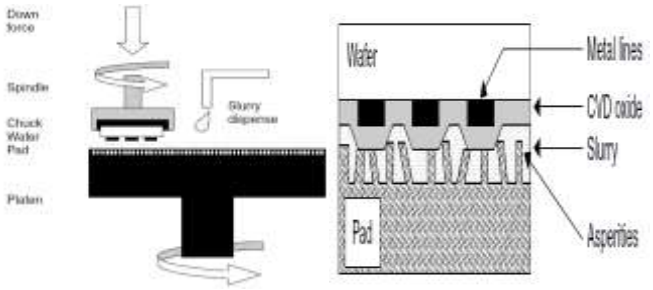


Fig. 6.4 Chemical Mechanical polishing

Pads are rough, with say 50μm roughness, and contact is made by asperities, and the contact area is only a fraction of the wafer area .Factors effecting chemical mechanical properties are structure height, mechanical properties of wafer, applying pressure etc. pad material is mainly used as polyurethane. Slurry incorporates both mechanical element with the help of abrasive particles and hardness .Slurry materials are silica and alumina. At the end of CMP a soft polishing step is needed for removing abrasive particles and corrosive chemicals. There are three modes in polishing they are direct contact mode, Non-contact mode &rolling contact mode. In direct contact mode pad makes direct contact with wafer resulting high friction because of no lubrication is applied by slurry [9]. In the rolling contact mode (mixed lubrication mode), slurry particles occasionally roll on the wafer surface. In the noncontact mode (hydrodynamic lubrication mode), slurry particles are accelerated hydro dynamically and they impart energy to the wafer surface, which leads to weakening of the surface so that chemical attack can occur. Hydrodynamic lubrication takes place at high velocities at which the load is borne by the fluid, and the system is well lubricated.

Rs. = (3/4) d (P /2kE) 2/3.

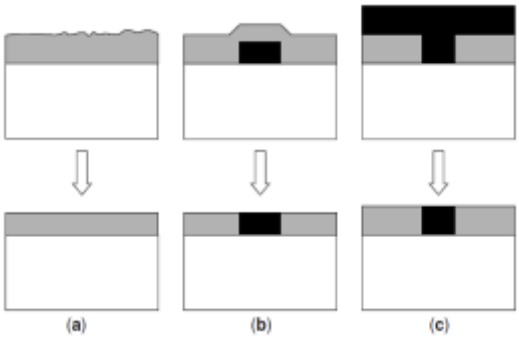


Fig. 6.5 Applications of polishing: (**a**) smoothing; (**b**) planarization and (**c**) damascene

Where d is the abrasive particle diameter (e.g., 100 nm), k is the filling factor of abrasive particles (for instance,50%), P is the local pressure (not down force, which is 10–50 KPa) and E is Young's modulus of the surface being polished. Penetration depths are of the order of nanometers, which is similar to surface roughness after polishing.

6.6 Bonding and layer transfer

Wafer bonding is a process of joining two wafers by the application of bond. Bonding create cavity and seals channel and enables highly 3D structure [10]. Two main classification of bonding are

1) Direct bonding

2) Indirect bonding

Direct bonding is process of chemical reaction (chemical bond) across the bonded surface. Oxidized silicon and glass wafers are commonly used in direct bonding. In direct bonding due to strong bonding interface breakages happens only inside the wafer not on the bonding surface.

The bonded wafers can be processed further as same as single wafer.

Indirect bonding uses great variety of materials such as glues. Indirect bonding should be processed at low temperature less than 400°C.glue limits the process temperature and ambient [11].

Layer transfer is the process of cutting or separating thin layers from substrate and transferred into another substrate. Most common method is the hydrogen bubble splitting. Hydrogen bubble–induced layer splitting is based on hydrogen implantation. Gas bubbles form at the depth of maximum hydrogen concentration. These bubbles lead to mechanical weakening of the silicon material, and micro cracks lead to cleavage of the implanted layer when suitable thermal treatment or mechanical pressure is applied. Hydrogen implantation method is patented, and called Smart-cut. Wafers manufactured with this method are marketed as Unibond.

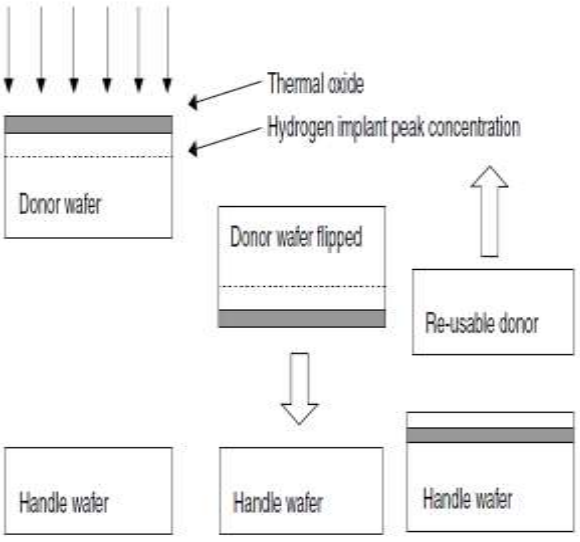


Fig. 6.6 layer transfer

7. EQUIPMENT FIGURES OF MERITS

Equipment figures of merit include various aspects such as process, capital cost, labour, consumables etc. Some of the most important ones are briefly explained below.

7.1 Uptime/downtime

` It is an overall measurement of equipment availability. The uptime is reduced both by scheduled and non-scheduled maintenance. Recalibration/test wafers requires to dismantle the process after running a long time which leads to down time of equipment .Regular reactor cleaning is a mandatory for deposition equipment and sometime chamber cleaning is also required for every wafer which leads to down time of equipment.

7.2 Utilization

It is a measure of equipment use that is, the actual productive hours of all available hours. General-purpose tools such as lithography have high utilization while the more dedicated tools have lower utilization.

7.3 Throughput

It is the no. of wafers per hour the system can handle. Single-wafer tools have throughputs of 25 to 50 WPH (wafer per hour), but batch tools can handle up to 200 WPH.

7.4 Foot Print

It is the size of clean room space. Normally the price of clean room space is $10 000 per square meter for class I clean room. In normal cases the front panel of system is in the clean room and rest of tool is in service area.

7.5 MTTF, MTBC

MTTF (Mean time between the failure) It is the time distance between the two tool failure. MTBC (mean time between cleaning) It is the process dependent. Particles are counted regularly and increase in the count requires cleaning.

7.6 Measurement of fabrication process

The different aspects of measuring the fabrication process are tool, process, and wafer. Tool parameters are RF power, mass flow rate, process time etc. A process measurement deals with ionic strength in a cleaning solution, electron and ion energies in plasma or anion dose.

Measurements can be classified into four categories

according to their immediacy:

– *in situ*: during wafer processing in the process chamber

– in-line: after wafer processing in the process tool (e.g., exit load lock)

– on-line: in the wafer fab by wafer fab personnel

– *ex situ*: outside the analytical laboratory by expert users

7.7 Devices

Micro fabricated device can be classified by many ways:

- Volume (or bulk) devices;
- Surface devices;
- Thin film devices;
- Stacked devices.

7.8 Volume devices

Power transistors, thyristors, radiation detectors and solar cells are comes volume devices. Currents are generated and transported (vertically) through the wafer. The starting wafers for volume devices need to be uniform throughout. Patterns are often made on both sides of the wafer and it are important to note that some processes affect both sides of the wafer and some are one sided.

7.9 Surface devices

In case surface devices make use the properties of substrate but generally only a fraction of wafer thickness is utilized in making the devices. Device structure or operation is connected with the properties of substrate. Most ICs fall under this category such as metal oxide semiconductor (MOS) and bipolar transistors, photodiodes and CCD image sensors.

7.10 Thin film devices

In case of thin film devices, product is built by depositing and patterning thin films on the wafers, and the wafer has no role in device operation. Wafer properties like thermal conductivity or transparency may be important, but the substrate is not machined or modified.

For example thin film transistors are made under this category.

7.11 Stacked devices

Stacked devices are made by layer transfer and bonding techniques. Two or more wafers are joined together permanently. Devices with vacuum cavities, such as absolute pressure sensors, accelerometers and gyroscopes are stacked devices made of bonded silicon/ glass wafer pairs. Micro pumps and valves, and many micro power devices like turbines and thrusters are stacked devices with up to six wafers bonded together.

8. CONCLUSION

Micro fabrication technologies originated from the microelectronics industry has now became an advanced technology for the manufacturing of miniature electro mechanical components. Its application include from common Integrated circuit to advanced bio-electro mechanical systems such as e genomics, proteomics, molecular diagnostics. Micro fabrication is the key element in the manufacturing of photo voltaic cells and other semi conducting devices. Micro fabrication involves many complex process and tools. It begins from Silicon preparation and end as finished product.

Micro fabrication is actually a collection of technologies which are utilized in making micro devices. The major processes are silicon wafer preparation, pattern generation, optical lithography, etching, ion implantation and bonding and layer transfer. These micro fabrication processes are carrying out under different micro fabrication tools. The cleanliness is key factor in all micro fabrication process. At the beginning and end of each process cleanliness should be done to avoid unwanted contamination which cause defects in the system. Different physical and chemical conditionings are employed at different stage of preparation. The process like Spin coating, Czochralski crystal growth etc are some of the main micro fabrication tools which are widely used for precision.

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