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IMPLEMENTATION OF WALLACE TREE MULTIPLIER USING CARRY SELECT ADDER WITH BINARY TO EXCESS-1 CONVERTER

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Abstract - *Multipliers are major blocks in the most of the digital and high-performance systems such as Microprocessors, Signal processing Circuits, FIR filters etc. In the present scenario, Fast multipliers with less power consumption are leading with their performance. Wallace tree multiplier with carry select adder (CSLA) is one of the fastest multipliers but utilizes more area. To improve the performance of this multiplier, CSLA is replaced by binary excess-1 counter (BEC) which not only reduces the area at gate level but also reduces power consumption. Area and power calculations for the Wallace tree multiplier using CSLA with BEC are giving good results compared to regular Wallace tree multiplier.*

Key Words: **Xilinx software, Binary to Excess one converter (BEC), Carry Select Adder (CSLA), Half Adder (HA), Full Adder (FA), Ripple Carry Adder (RCA), Multipliers.**

1. INTRODUCTION

A processor is the substantial block, in which the performances accelerate along with the processor speed of the system. The performance of the processor mainly depends on the multiplier as most of the processors time depends on the multiplication process. Major applications like VLSI, digital signal processing requires high performing processors to obtain the processing of huge amount of data. Multiplier architecture consists of three stages, partial products generation stage these are generated by AND operation, partial products addition stage carried by different adders and final addition stage. Speed plays the major role in many of the multipliers. To reduce the delay and to accelerate the multiplication, the number of partial products is reduced. Wallace tree multiplier is designed with CSLA in order to increase the speed. The importance of BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

2. LITERATURE SURVEY

2.1 Two-bit BEC

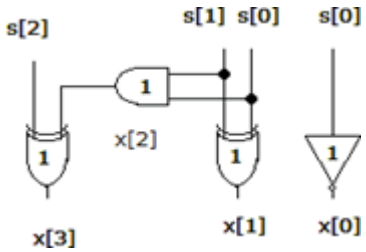

Fig.1.Binary to Excess-1 Converter

In regular CLSA as the utilization of gates are more due to this power consumption also increases. Now by using BEC in regular CSLA we can reduce number of gates and simultaneously decreases power consumption. For two-bit BEC first s (0) is given to the NOT gate to obtain x (0). Next s (0), s (1) are given input for the XOR and AND gate to obtain sum x (1), carry x (2). Next x (2), s (2) are given to XOR gate to generate sum x (3).

2.2. Wallace tree Multiplier for 4-bit

Step by step procedure for multiplying two four-bit integers according to Wallace multiplier.
Wallace multiplier consists of three steps:

1. Multiply each bit of one argument with each bit of another argument, which results in n^2 products.
2. Consider the first three rows of the multiplied products and reduce them into two rows by using full adders and half adders as per the requirements. Repeat this process until two rows of multiplied products are obtained.
3. Normally in the case of four-bit additions of two integers a sum of four bits and carry one bit is formed. So, in the last step of layer we first have two

rows of products half adder to add last two bits and the carry of the half adder is connected to the next layer. By following the same procedure add all the bits of two rows. At last the sum of four bits can be obtained

Coming to the solution of 4*4 Wallace tree multiplier, in first stage we obtain four rows of the multiplied products as shown in the Fig. 1.

```
                        a3  a2  a1  a0
                        b3  b2  b1  b0
-------------------------------------------
                    a3b0  a2b0  a1b0  a0b0
                a3b1  a2b1  a1b1  a0b1
            a3b2  a2b2  a1b2  a0b2
        a3b3  a2b3  a1b3  a0b3
```

Fig.2.Partial Products Generation

Now in the second stage choose the first three rows and reduce them into two rows by using half adders and full adders. As per the requirement it is needed two half adders and two full adders, sum and carry are generated as a0b0, s(0)c(0), s(1)c(1), s(2)c(2), s(3)c(3), a3b2 as in the Fig.2.

```
                a3b0  a2b0  a1b0  a0b0
            a3b1  a2b1  a1b1  a0b1
        a3b2  a2b2  a1b2  a0b2
-------------------------------------
        a3b2  s3    s2    s1    s0    a0b0
        c3    c2    c1    c0
```

Fig.3.Partioning and Addition of the Partial Products for Group1

These obtained products are added to the fourth row of the multiplied products in the third stage by this operation the results of sum and carry as a0b0, s(0), s(4)c(4), s(5)c(5), s(6)c(6), s(7)c(7), a3b3 are obtained here one half adder and three full adders are used, It is shown in Fig.3.

```
            a3b2  s3    s2    s1  s0  a0b0
            c3    c2    c1    c0
        a3b3  a2b3  a1b3  a0b3
-------------------------------------
        a3b3  s7    s6    s5    s4  s0  a0b0
        c7    c6    c5    c4
```

Fig.4. Partioning and Addition of the Partial Products for Group2

Finally in the fourth stage again add this sum and carry to obtain the last stage products as a0b0, s(0), s(4), s(8), s(9), s(10), s(11)c(11),two half adders and three full adders are used in this stage as shown in the below Fig.4.

```
a3b3    s7    s6    s5    s4    s0    a0b0
c7      c6    c5    c4
c10     c9    c8
-------------------------------------------
c11 s11 s10   s9    s8    s4    s0    a0b0
```

Fig.5. Partioning and Addition of the Partial Products for Group3

2.3. Carry Select Adder (CSLA)

The carry-select adder generally consists of ripple carry adder and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple-carry adders), in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.

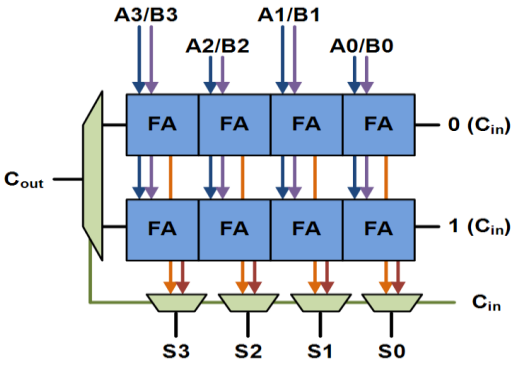

Fig.6.Carry select adder

2.4. Xilinx ISE

Xilinx ISE (**I**ntegrated **S**ynthesis **E**nvironment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to compile their designs, perform timing, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the Programmer. Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or the model sim logic simulator is used for system-level testing.

3. BLOCK DIAGRAMS

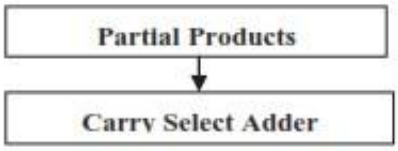

Fig.7.Block diagram for Wallace tree multiplier using CSLA

Partial products obtained from the group 2 were given to the carry select adder, as this addition process reduces the delay as compared with the normal Wallace tree multiplier to generate the final multiplication products

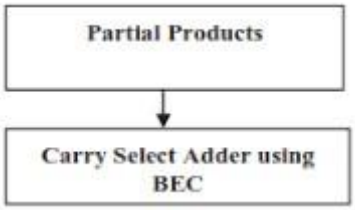

Fig.8. Block diagram for Wallace Tree Multiplier using BEC

Partial products obtained from the group 2 were given to the carry select adder using BEC in order to reduce the delay and it uses a smaller number of gates when compared to the Wallace tree multiplier using CSLA, and obtain the final products of the multiplication.

4. RESULTS

Wallace Multiplier is synthesized using XILINX ISE Design Suite 14.2 and is implemented on FPGA device xc3s500-5fg320 of Spartan 3E family.

The Input output waveforms which are generated by using XILINX software and device utilization summary are shown.

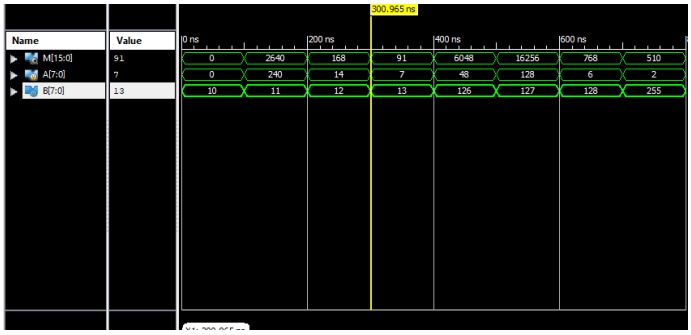

Fig.9. simulation result for Wallace tree multiplier

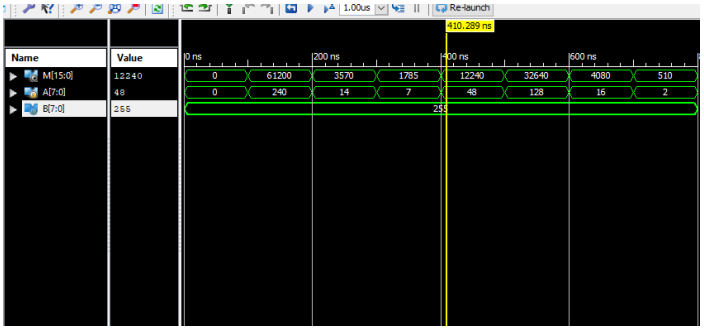

Fig.10. simulation result for Wallace tree multiplier using CSLA

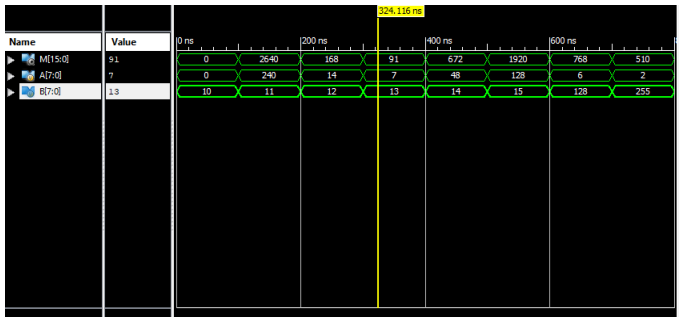

Fig.11. simulation result for Wallace tree multiplier using CSLA with BEC

Parameters	Wallace tree multiplier	Wallace tree multiplier using CSLA	Wallace tree multiplier using CLSA with BEC
Memory(kB)	4695376	4445252	4445064
Delay(ns)	5.054	4.909	4.909
Power(mW)	43.22	42.88	40.98

Table.1. Comparison of Wallace tree multiplier using CSLA and BEC

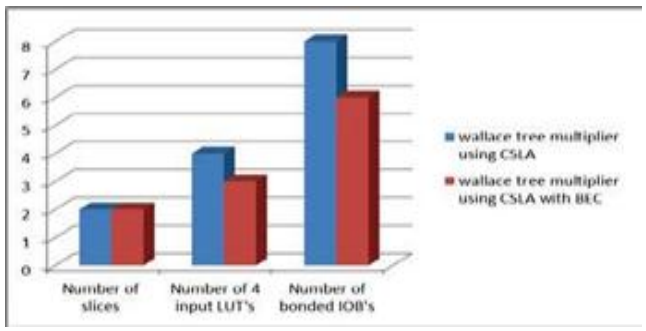

Fig.12. Chart indicating area parameters for Wallace tree multiplier using CSLA and Wallace tree multiplier using CSLA with BEC

Number of slices for RCA in CSLA is two, whereas number of slices in BEC is two. Number of 4 input LUT's for RCA in CSLA is four and number of inputs LUT's in BEC is three.

Number of bonded IOB's for RCA in CSLA is eight and in case of using BEC is six. From these observations of area parameters, it is clear that area utilization in Wallace tree multiplier using CSLA with BEC is area efficient.

5. CONCLUSION

A Simple approach is proposed in this paper to reduce the area of Wallace tree multiplier using CSLA. From the above results it is observed that the Wallace tree multiplier using CSLA with BEC is occupying less area, memory and consuming less power when compared to Wallace tree multiplier using CSLA and Wallace tree multiplier.

6. REFERENCE

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