

Analysis of Carrier based PWM Controlled Modular Multilevel Converter based VFD without Intermediate DC bus

Mr. Sachin Kapadiya¹, Mr. Arpan Patel², Mr. Kaumil Shah³

^{1,2}Post Graduate Student, Dept. of Electrical Engineering, S. K. Patel University, Gujarat, India ³Professor, Dept. of Electrical Engineering, S. K. Patel University, Gujarat, India _____***_____

Abstract - The multilevel inverters have received extensive importance in crucial applications because of low total harmonic distortion and low switch stress. With advantageous features such as modularity, scalability, multilevel waveform, no dc link, lower harmonic spectrum, and cost-saving a Modular Multilevel Converter (MMC) is suitable for high voltage, high power applications such as HVDC, MV VFD, static compensator, unified power quality conditioners, etc. The work presented here focuses on utilizing Half-bridge submodule based Modular Multilevel Converter for variable frequency drive without an intermediate DC bus between rectifier and inverter. A high-frequency multi carrier PWM switching technique namely Phase-shift carrier (PSCPWM) modulation is used for switching of converter cells.

Key Words: Modular Multilevel Converter, Voltage Balancing, MMC, Phase shift PWM, VFD, DC bus.

1. INTRODUCTION

In the current era of technology and advancement, the global demand for clean energy is increasing rapidly. A future seems energy-hungry. One of the solutions which is under investigation and implementation is increasing the energy efficiency of end-user applications and consumers [1]. A young modular multilevel converter technology support sustainability goals by enabling the cost-efficient, reliable and energy-efficient application control at the end-user side. Among all types of load, the induction motors in industries are the most used machine with its wide range of applications. Variable Frequency Drive (VFD) is a power electronics circuitry/device which gives full control over the industrial motor.

1.1 MMC based VFD configuration

The first stage of the variable frequency drive is the rectifier. It converts ac energy to dc energy.



Fig -1: MMC based VFD with DC bus

The second stage of the variable frequency drive is the inverter. It does the reverse, converts dc energy to ac. Inverter control speed and torque of motor by controlling

voltage and frequency to the motor. MMC based VFD is shown in Fig-1. A proposed MMC based VFD without DC bus capacitors is shown in fig-2.



Fig -2: MMC based VFD without DC bus

1.2 MMC configuration

MMC is a modular structure-based power converter. The half-bridge submodule consists of one two-level phase leg parallel to a dc capacitor that will maintain a direct voltage [2]. It employs a cascade connection of submodules to reach the desired system voltage while producing a high-quality multilevel output voltage waveform [3]. The external terminals of the submodule are formed by the phase leg midpoint on the one hand and one of the dc capacitor terminals on the other hand [2]. While connecting cells in cascade a capacitor terminal of one submodule go to midpoint terminal of the next submodule and so on. A threephase MMC converter, submodule and cascade connection of submodules is illustrated in fig-3.





1.2 Submodule switching states

Two possible switching states are possible [2]. In the first, called bypass, the switch in the valve parallel to the external terminal is conducting and the terminal voltage is zero [2]. In the other state, labeled insertion, the valve in series with the

submodule capacitor is conducting, implying that the voltage at the terminal equals the capacitor voltage [2].



Table -1: Submodule operation states

1.2 Passive components of MMC

The arm inductor is a passive component used in MMCs. The arm inductor is connected in series with each group of submodules to limit the current due to the instantaneous voltage difference between the arms [3]. Arm inductance limits DC short-circuit current and filters the switching frequency harmonics. Therefore, sizing of the arm inductor depends on the arm current ripple and short-circuit current [4]. The suppression of undesirable low-frequency currents needs to be considered during the design of an arm inductor [4]. Formula to determine arm inductance from [6],

$$L_0 = \frac{1}{8 \cdot C_0 \cdot \omega_0^2 \cdot V_C^2} \left[V_{dc} + \left(\frac{P_s}{3 \cdot I_{2f}} \right) \right]$$
(1.1)

Where, L_0 =Inductance, C_0 =Number of capacitors in the arm, P_s=Apparent Power KVA, ω_0 =Fundamental frequency Hz, V_{SM} =Submodule voltage, V_{dc} =DC bus voltage.

The submodule capacitor is sized based on the tradeoff between the size or cost and capacitor voltage ripple [4]. It is designed to provide a permissible peak-to-peak ripple at twice the fundamental frequency [4]. The submodule capacitors voltage must be regulated at the given reference voltage value to produce a multi-level stepped waveform at the output of MMC. The MMC has several submodules in each arm and controlling all these submodules is one of the challenging tasks. The capacitor voltage control is usually separated into three stages named as, leg voltage control, voltage balance among the arms, and voltage balance among the submodules within the arm [4]. A circulating current exists within each phase-leg of the MMC and has a significant impact on the ratings of the power devices, capacitors voltage ripples and power losses [5]. Capacitor voltage balancing can be implemented at either the control stage or the modulation stage. The capacitor voltage balancing is also required to keep the capacitors voltages at the reference value [5]. Formula to determine submodule capacitance from [7],

$$V_{SM} = \frac{V_{dc}}{n}$$
(1.2)

$$V_{dc} = 1.414 \cdot V_{ac}$$
 (1.3)

$$n = \frac{(m-1)}{2}$$
 nos. (1.4)

$$C_{SM} = \frac{P_{S}}{3 \cdot K \cdot n \cdot \omega_{0} \cdot V_{SM}^{2} \cdot s} \left[1 - \left(\frac{\cos\varphi}{2}\right)^{2} \right]^{3/2} \quad (1.5)$$

K= Modulation index, $\cos \varphi$ =Power factor, n=Number of modules in the arm, V_{SM} =Submodule voltage, ε =Submodule voltage ripple V

2. SIMULATION

A simulation modular multilevel converter based VFD is performed using a simulation tool named PSIM. The following data is considered for simulation: Input 3-phase, 50Hz, 415Vac, DC bus capacitance, and module capacitance value 4700uF, Arm inductance 10mH, Number of the submodule in one phase 8. RL load equivalent to the induction motor. A simulation is performed for with PSCPWM switching technique and capacitor voltage balancing program.

2.1 Modulation technique

A wide range of modulation techniques can be applied to the MMC, mainly depending on the number of SMs in the phaselegs of the converter. The most common ones are carrierbased PWM [5]. The modulation scheme with the horizontal disposition of identical triangular carrier signals is referred to as phase-shifted carrier modulation (PSC-PWM) [3]. PSCPWM illustrated in fig.4. All triangular signals have the same frequency and peak-to-peak amplitude, but there is a phase-shift between the adjacent triangular signals [3]. A require with Phase shift in one arm,

$$\phi_c = \frac{360}{n} \tag{2.1}$$



International Research Journal of Engineering and Technology (IRJET)

www.irjet.net

e-ISSN: 2395-0056 p-ISSN: 2395-0072



Volume: 07 Issue: 04 | Apr 2020

2.2 Capacitor voltage balancing algorithm

A common way to perform capacitor voltage balance is based on sorting the capacitor voltage values from the highest to the lowest or vice versa, and making a decision on the SMs to be activated/deactivated considering the direction of the arm current [5]. When the number of activated SMs within an arm increases, the SMs with lowest/highest voltages will be activated if the current direction is such that it charges/discharges the capacitors [5]. First measured all submodule capacitor voltages of one leg and generate an array in program. Then sort those values in ascending/descending order in array. Then, Insert or bypass the submodule according to the PWM requirement depending on the arm current direction. Below is the summary table for activating/deactivating of SM.

 Table -2: SM voltage balancing conditions

Arm current direction	PWM requirement	Identify SM with voltage level
Charging (+ve)	Addition	Lowest
	Removal	Highest
Discharging (-ve)	Addition	Highest
	Removal	Lowest

3. SIMULATION RESULT





Fig -5: Simulation results with DC bus (*a*) Line to Line output voltage, (*b*) Submodule capacitor voltages, (*c*) Output current, (*d*) Output voltage harmonics





International Research Journal of Engineering and Technology (IRJET) e-ISSN: 23

Volume: 07 Issue: 04 | Apr 2020

www.irjet.net



Fig -6: Simulation results without DC bus (*a*) Line to Line output voltage, (*b*) Submodule capacitor voltages, (*c*) Output current, (*d*) Output voltage harmonics (e) Output current harmonics

Table -3:	Result	Table
-----------	--------	-------

Parameter	With DC bus	Without DC bus
VL	560 V	553 V
SM V _{Cap.}	145-147 V	140-143 V
V THD	27.2%	27.3%

3. CONCLUSIONS

The presented work compared the MMC based VFD with an intermediate DC bus and without an intermediate DC bus is performed. The Output voltage is within acceptable limit for

MMC without DC bus. From the results it is observed that voltage harmonics and current harmonics are nearly the same for both cases. With the same performance, the overall cost of MMC based VFD is reduced.

REFERENCES

- [1] Kamran Sharifabadi; Lennart Harnefors; Hans-Peter Nee; Staffan Norrga; Remus Teodorescu, "Introduction," in Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems, IEEE, 2016, pp.1-6.
- [2] Kamran Sharifabadi; Lennart Harnefors; Hans-Peter Nee; Staffan Norrga; Remus Teodorescu, "Introduction to Modular Multilevel Converters," in Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems, IEEE, 2016, pp.7-59.
- [3] Sixing Du; Apparao Dekka; Bin Wu; Navid Zargari, "Fundamentals of Modular Multilevel Converter," in Modular Multilevel Converters: Analysis, Control, and Applications, IEEE, 2018, pp.37-78.
- [4] Sixing Du; Apparao Dekka; Bin Wu; Navid Zargari, "Review of High-Power Converters," in Modular Multilevel Converters: Analysis, Control, and Applications, IEEE, 2018, pp.1-36.
- [5] R. Darus, J. Pou, G. Konstantinou, S. Ceballos and V. G. Agelidis, "A modified voltage balancing sorting algorithm for the modular multilevel converter: Evaluation for staircase and phase-disposition PWM," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 255-260.
- [6] M. Zygmanowski, B. Grzesik and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, 2013, pp. 1-10.
- [7] Qingrui Tu, Zheng Xu, H. Huang and Jing Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based HVDC," 2010 International Conference on Power System Technology, Hangzhou, 2010, pp. 1-6