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A Novel Simulated Analysis of Enhanced Carry Increment Adder using Various Adder Techniques

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Abstract - *A complex digital circuit has adder as a basic and important unit. Overall circuit performance will depend on the design of the adder circuit. So, if we reduce the delay of the adder unit then overall circuit delay will reduce. Thus speed of the overall circuitry will also get increased. In this paper we have compared the delay and area of CIA (carry increment adder) using different adder combinations. The improvement in the circuit performance is analyzed by incorporating various combinations possible in the design of RCA, CLA, HCA (Han-Carlson adder) and KSA (Kogge-Stone adder) along with LFA (Ladner-Fischer Adder) and BSA (Beaumont-Smith Adder). A synthesis study is done in terms of delay and area which is carried out for comparative analysis. Simulations and synthesis are done in Xilinx ISE 14.7 version and coding is done in Verilog HDL.*

Key Words: **BSA, CIA, CLA, delay, HCA, KSA, LFA, RCA.**

1. INTRODUCTION

Adder is one of the essential blocks in any digital system. Adder circuitry is useful in VLSI system like design of multiplier, ALU, DFT, IIR, FIR and in DCT filters as well as used in Wireless communication and DSP applications. In the recent years due to the fast growing technologies in mobile communication and computation, the demand for building low-power VLSI systems has also increased. The need of small and portable device is increasing rapidly which is possible due to VLSI. The performance of the VLSI system depends mainly on reduced delay, low power consumption, less area. The main component of ALU is the binary adder. An efficient adder is one that improves the performance of the adder circuit. In binary adder, speed is mainly dependent on the time it takes for propagating the carry through the adder. Over the last decade many different adder circuitries for improving the design has been done. In this project our main aim is to improve the performance of the Carry Increment Adder (CIA) circuitry by reducing the delay and area.

2. BASIC CARRY INCREMENT ADDER

A Basic Improved CIA consists of ripple carry adder and incremental circuit. Incremental circuit is designed using half adder and is connected one after the other with a consecutive order. Here we consider 8 bit Ripple Carry Adder (RCA) for analysis. In this circuit, we can divide the 8 bits into a group of 4 bit and addition is performed by two 4-bit RCA and is followed by increment circuitry that can generate the sum bit. After that final carry from incremental circuit and the output carry generated from second RCA will act as an input to OR gate. Thus, generate final output carry. The Carry Increment Adder is shown in Figure 1.

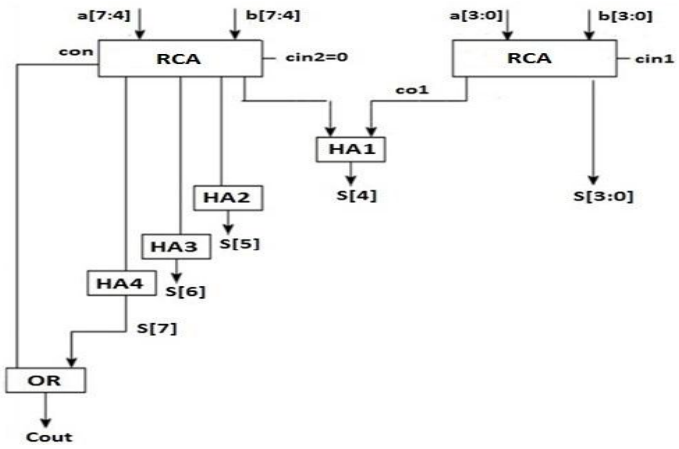

Fig -1: Basic 8-Bit Carry Increment Adder

2.1 Ripple Carry Adder

Ripple Carry Adder is a structure of multiple full adders is cascaded in a manner to gives the results of the addition of an n bit binary sequence. This adder includes cascaded full adders in its structure. Thus the carry will be generated at every full adder stage in a ripple-carry adder circuit. These carry output at each full adder stage is forwarded to its next full adder and there applied as a carry input to it. This process continues up to its last full adder stage. So, each carry output bit is rippled to the next stage of a full adder. The most important feature of it is to add the input bit sequences whether the sequence is 4 bit or 5 bit or any bit.

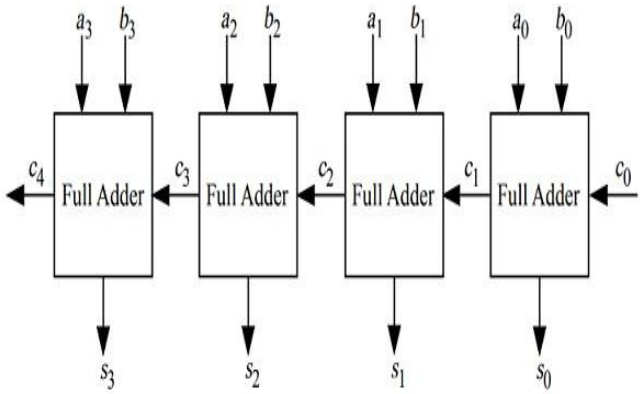

Fig -2: Ripple Carry Adder (4-Bit)

2.2 Limitations

A. Propagation delay is more in RCA as each full adder must wait for carry coming from previous adder.

B. This complicates CIA computation as well because of already existing delay due to ripple carry chain in incremental circuit.

3. ENHANCED CARRY INCREMENT ADDER

As explained in the previous section, the architecture flow remains the same but the adder used as a base can be changed in order to achieve better performance and thus comparison is being made. The Enhanced Carry Increment Adder consists of different adder combinations and incremental circuit. Incremental circuit is designed using half adder and is connected one after the other with a consecutive order. The Different adder combinations are referred to as 4-bit adder which may be same or different in the given figure.

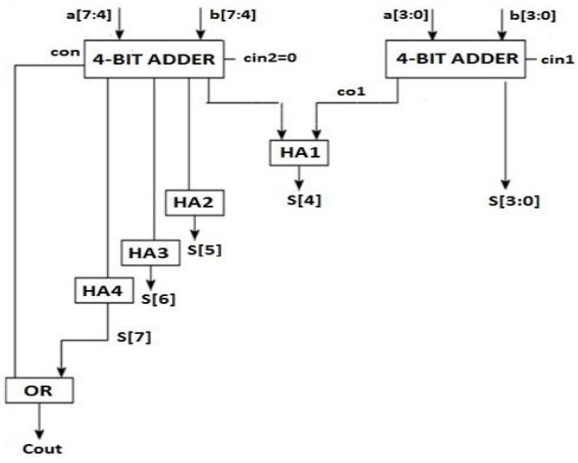

Fig -3: Enhanced 8-Bit Carry Increment Adder

3.1 Carry Increment Adder with Carry Look-Ahead Adder

Basic CIA with RCA i.e., CIA_RCA is a good fast adder and very simple to design but it has its disadvantage that in RCA delay is more compared to Carry Look-Ahead Adder(CLA) due to which delay of the entire circuit has been increased, thus it affects the performance of the circuit. Now for identifying better Performance of CIA, We have made changes in CIA_RCA circuit by substituting the RCA with CLA block and remaining circuit is same.

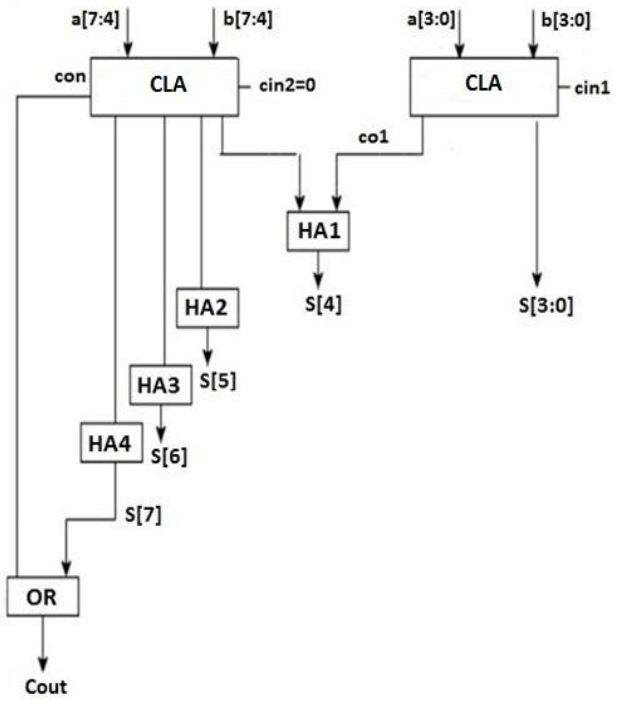

Fig -4: Carry Increment Adder (8-Bit) With CLA

3.1.1 Carry Look-Ahead Adder

CLA improves the speed by reducing the computation time. In CLA, addition operation occur by producing two signals Propagate and Generate based on whether a carry is generated when both inputs are 1 or propagated through less significant bit position when at least one input is 1 or killed when together inputs is 0. In CLA Propagate is the output sum of HA and Generate is output carry of the adder. When Propagate and Generate is generated then the carry is created to each position of a bit.

The Propagate and Generate Bits are
Pi = ai (xor) bi
Gi = ai (and) bi

Thus the Sum and Carry bits are given by
Si = Pi (xor) ci
ci+1 = Gi (or) [Pi (and) ci]

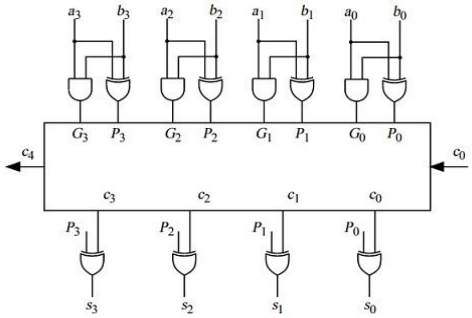

Fig -5: Carry Lookahead Adder (4-Bit)

3.2 Carry Increment Adder with Parallel Prefix Adders

For further reducing the delay in CIA, Parallel Prefix Adders (PPA) can be used instead of RCA and CLA. Thus, the speed of the total circuitry gets increased. As parallel prefix adders can be used in complex circuit in which adder circuitry is used as a basic adder unit for reducing the delay of the circuit.

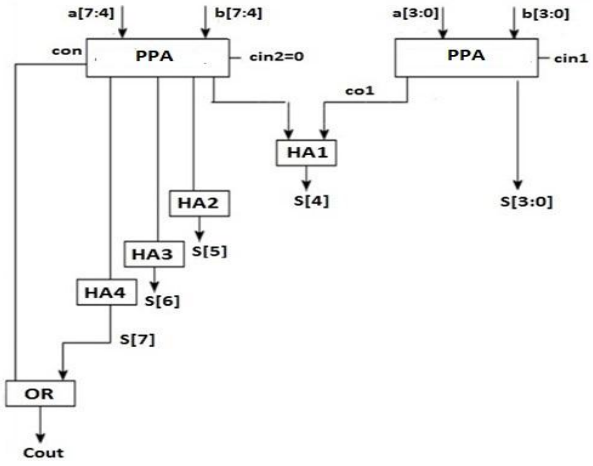

Fig -6: Carry Increment Adder (8-Bit) With PPA

3.2.1 Kogge-Stone Adder

The Kogge-Stone Adder is a Parallel Prefix form of Carry Look-Ahead Adder. This adder is widely used in the industry and considered as the fastest adder design. Every column stage produces both propagate as well as generate signals. Generate signals which are calculated in the final stage are made XOR with initially produced propagate and generate signals to produce sum. The advantage in Kogge-Stone adder is that it generates carry bits in O (log2 n) time delay complexity. It reduces the critical path to great extent so that it increases its performance in implementing higher bit adders. Kogge-Stone Adder takes greater area for implementing but it has lesser fan-out (Maximum fan-out=2). The major disadvantage of this adder is Wiring Congestion.

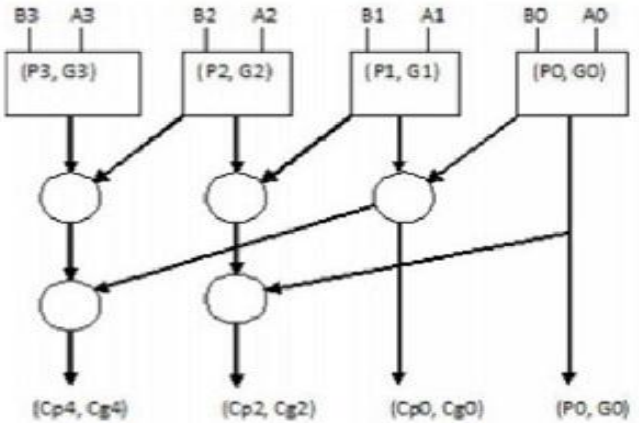

Fig -7: Kogge-Stone Adder (4-Bit)

3.2.2 Ladner-Fischer Adder

Ladner-Fischer adder is another parallel prefix form carry look-ahead adder. A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. It is a fastest adder design and common design for high performance adders in industry. The better performances of Ladner-Fischer adder are minimum logic depth and bounded fan-out. But it has large area.

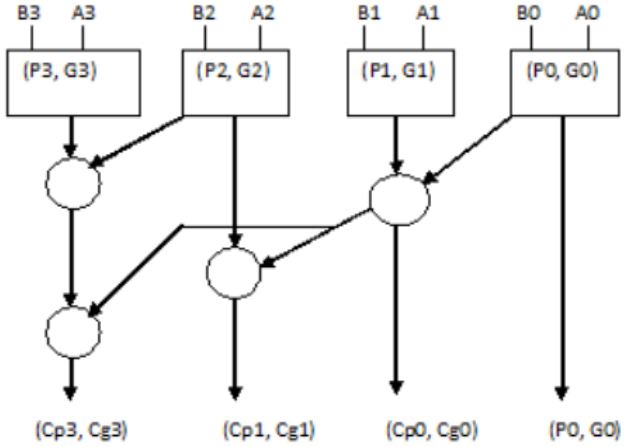

Fig -8: Ladner-Fischer Adder (4-Bit)

3.2.3. Han-Carlson Adder

Han-Carlson adders are popular choice in high speed ALU architecture. Han-Carlson is a parallel prefix adder having an advantage of providing higher speed and low area. Carry generation of Han-Carlson Adder normally involves 2 types of stages. Central stages are same as Kogge-Stone Adder tree structure. The remaining stages involve Brent-Kung Adder tree computation. This adder uses less Black cells and it has shorter wire complexity than Kogge-Stone Adder. The complexity can be reduced at the cost of an extra stage for carry merge path.

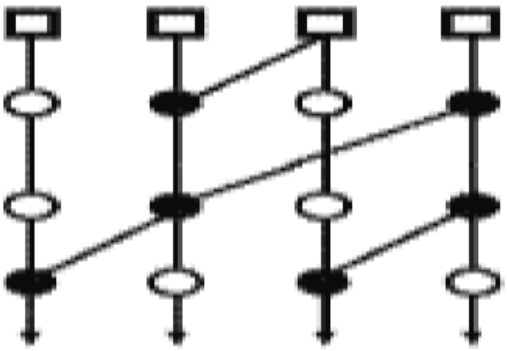

Fig -9: Han-Carlson Adder (4-Bit)

3.2.4 Beaumont-Smith Adder

Beaumont-Smith adder is a parallel prefix adder determined to solve the disadvantages of Ladner-Fischer adder. The cost and wiring complexity is greatly reduced. But the logic depth of Beaumont-Smith adders increases to 2log (2n-1), so the speed is lower. These adders are critically important in processor chips. They are used in floating point Arithmetic units, memory addressing, and program counter up data. They are mainly responsible for setting the minimum clock cycle in processor. They are mostly efficient in power consumption and chip area.

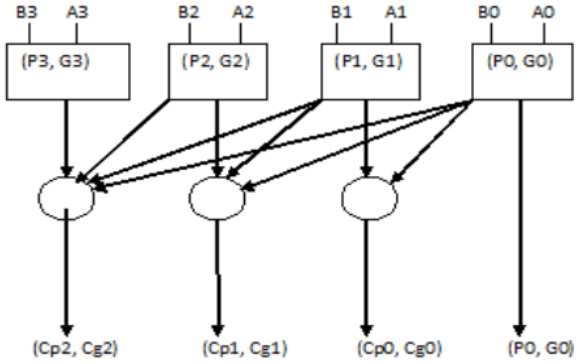

Fig -10: Beaumont-Smith Adder (4-Bit)

3.3. Carry Increment Adder with Different Combinations

Each and every adder techniques combine with each other so as to provide a better performance adder that will help in processing data quicker for different applications. The Different Combinations of CIA are listed as RCA Combination, CLA Combination, KSA Combination, HCA Combination, LFA Combination and BSA Combination.

4. RESULTS AND DISCUSSION

The Comparative simulation analysis of the proposed Carry Increment Adder architecture is presented in this chapter. The RTL code is written using Verilog HDL and the simulation and design synthesis is carried under Xilinx ISE 14.7 environment. The Adder Techniques used were analyzed first and tabulated as below.

Table -1: Adder (4-bit) Comparison

ADDERS USED	DELAY(ns)	NUMBER OF SLICES(3584)	NUMBER OF LUTS(7168)
RCA	13.902	4	8
CLA	13.775	4	8
KSA	13.775	4	8
HCA	12.075	5	9
LFA	13.648	4	8
BSA	13.775	4	8

We have performed the experiment for addition of 8 bit binary numbers. Out of all the experiments that were conducted, Han-Carlson Combination (direct) provides a better performance based on both area and delay. The best performing CIA combinations are listed as HCA-RCA, HCA-CLA, HCA-KSA and HCA-BSA.

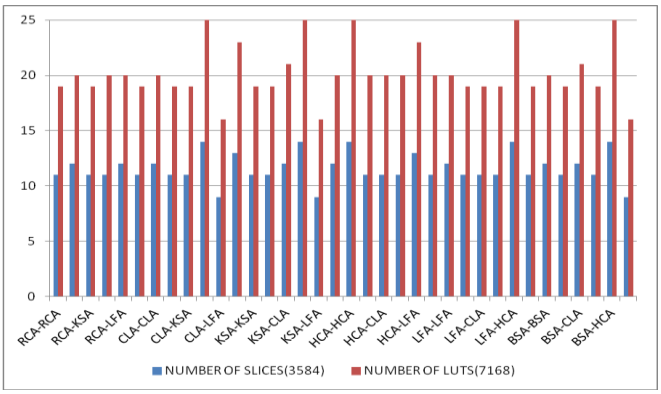

Chart -1: Area Comparison of CIA

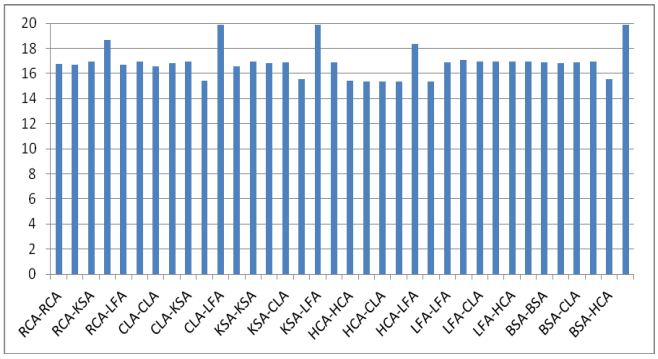

Chart -2: Delay Comparison of CIA

5. CONCLUSION

Thus from the above experimentation, CIA circuit with Han-Carlson adder combination presented a reduction in complex circuitry in comparison to other adder combination in terms of delay. Also CIA with Ladner-Fischer adder combination provides better area in comparison. Thus if we use CIA with Han-Carlson adder combination as a basic adder unit in a complex circuitry then overall speed of the complex circuitry gets improved as CIA with Han-Carlson adder combination has less delay as compared to other adder circuitry. Thus, depending on the necessary applications we can use the specific adder.

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