

DESIGN OF LOW POWER HIGH SPEED FULL ADDER CIRCUITS USING XOR-XNOR TOPOLOGY

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Abstract- The explosive growth of battery operated portable applications such as cellular phones, smart cards, PDAs, laptops and the evolution of the shrinkage of the technology requires smaller silicon area, high throughput circuitry and most importantly low power. Power consumption of any system can be reduced by scaling the supply voltage and operating frequency. But, it increases the propagation delay of the system and degrades the driving capability of the design. Therefore, designing a full adder with improved power delay characteristics is of great interest. The greatest challenge in low power VLSI design is reduction of power dissipation. Novel circuits for XOR/XNOR and simultaneous XOR-XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption. The proposed circuits are investigated in terms of variations of the supply and threshold voltages, output capacitance, input noise immunity, and the size of transistors. The simulations are carried out in Tanner EDA tool.

Key Words: CMOS, Low power VLSI, Full Adder, XOR-XNOR, Tanner EDA, Virtual ground.

1. INTRODUCTION

TODAY, ubiquitous electronic systems are an inseparable part of everyday life. Digital circuits, e.g., microprocessors, digital communication devices, and digital signal processors, comprise a large part of electronic systems. As

the scale of integration increases, the usability of circuits is restricted by the augmenting amounts of power and area consumption. Therefore, with the growing popularity and demand for the battery-operated portable devices such as mobile phones, tablets, and laptops, the designers try to reduce power consumption and area of such systems while preserving speed. Optimizing the W/L ratio of transistors is one approach to decrease the power-delay product (PDP) of the circuit while preventing the problems resulted from reducing the supply voltage. The efficiency of many digital applications appertains to the performance of the arithmetic circuits, such as adders, multipliers, and dividers. Due to the fundamental role of addition in all the arithmetic operations, many efforts have been made to explore efficient adder structures, e.g., carry select, carry skip, conditional sum, and carry look-ahead adders. Full adder (FA) as the fundamental block of these structures is at the center of attention. Based on the output voltage level, FA circuits can be divided into full-swing and non full-swing categories. Standard CMOS complementary pass transistor logic (CPL) transmission gate (TG) transmission function 14T (14 transistors), 16T and hybrid pass logic with static CMOS output drive full adder (HPSC). FAs are the most important full-swing families. Non full-swing category comprises of 10T, 9T, and 8T.

In this paper, we evaluate several circuits for the XOR or XNOR (XOR/XNOR) and simultaneous XOR and XNOR (XOR-XNOR) gates and offer new circuits for each of them. Also, we try to remove the problems existing in the investigated circuits.

Afterward, with these new XOR/XNOR and XOR-XNOR circuits, we propose six new FA structures. The circuits for XOR/XNOR and simultaneous XOR-XNOR are reviewed, novel XOR/XNOR and XOR-XNOR circuits are proposed and the

simulation results of these structures are presented. In the transistor sizing methods are first investigated and the circuits are simulated for power, delay, and PDP parameters. The simulation results are analyzed and compared.

2 PROPOSED DESIGN

In this paper the circuits are designed using novel XOR-XNOR circuit. One of the important factors is that excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multichip module. Unless power consumption is dramatically reduced, the resulting heat will limit the feasible packing and performance of VLSI circuits and systems. So XOR-XNOR circuit is in-cooperated in digital circuits to reduce the power consumption.

2.1 INVERTER

An inverter circuit outputs a voltage representing the opposite logic-level to its input. Inverters can be constructed using two complementary transistors in a CMOS configuration. This configuration greatly reduces power consumption since one of the transistors is always off in both logic states.

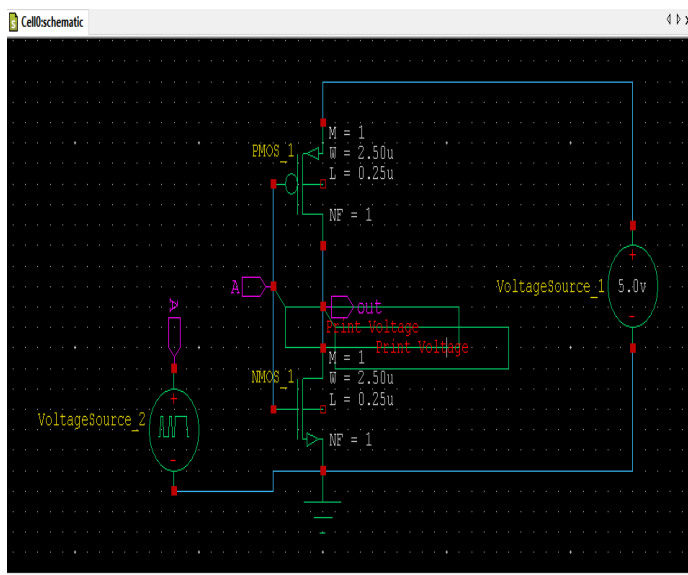


Fig-1: Inverter circuit

The proposed XOR and XNOR circuits are based on the modified version of a CMOS inverter and pass transistor logic. In proposed circuit-I, for XOR when the input B is at logic 1, the inverter circuit functions like a

normal CMOS inverter. Therefore, the output is the complement of input A.

2.2 CMOS HALF ADDER

Adders are used in processors in the arithmetic logic units, to calculate addresses, table indices, and other similar operations. A fast and energy-efficient adder plays a vital role in electronics industry. Adder contributes substantially to the total power consumption of the system. Half Adders are frequently required in VLSI from processors to application specific integrated circuits (ASICs). Adder circuit is a combinational digital circuit that is used for adding two numbers. A typical adder circuit produces a sum bit (denoted by S) and a carry bit (denoted by C) as the output. Typically adders are realized for adding binary numbers but they can be also realized for adding other formats like BCD (binary coded decimal, XS-3 etc. Besides addition, adder circuits can be used for a lot of other applications in digital electronics like address decoding, table index calculation etc. For more than four decades, downscaling of CMOS has been the fundamental strategy for improving the performance of VLSI circuits.

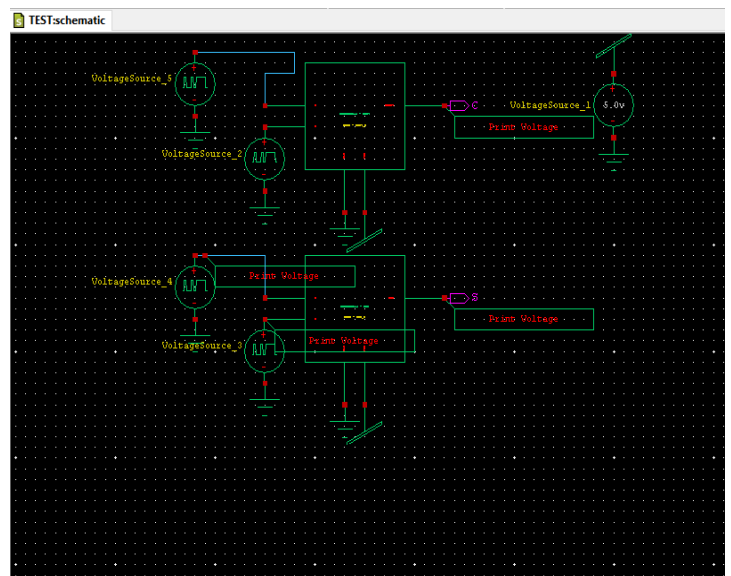


Fig-2: CMOS Half adder

In DSPs, and, versatile microprocessor, the wide-bit addition is vital in many applications such as ALUs, multiply-and accumulates (MAC) units. The half adder adds two single binary digits A and B. It has two outputs, sum (S) and carry (C). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is A+B. The simplest half adder design incorporates an XOR gate for S and an AND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The half adder adds two input bits and generates a carry and sum, which are the two outputs of a half adder.

2.3 XOR-XNOR CIRCUIT

Hybrid FAs are made of two modules, including 2-input XOR/XNOR (or simultaneous XOR–XNOR) gate and 2-to-1 multiplexer (2-1-MUX) gate. The XOR/XNOR gate is the major consumer of power in the FA cell. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design. Many circuits have been proposed to implement XOR/XNOR gate which a few examples of the most efficient ones.

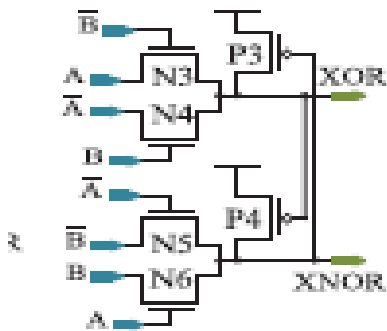


Fig-3: XOR-XNOR circuit

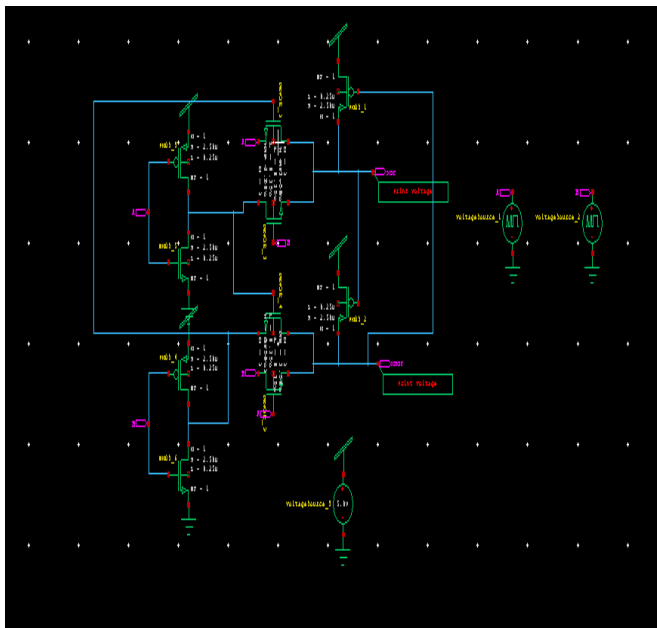


Fig-4 :XOR-XNOR circuit

The main problem of this circuit is using two high power consumption NOT gates on the critical path of the circuit, because the NOT gates must drive the output capacitance. Therefore, the size of the transistors in the NOT gates should be increased to obtain lower critical path delay. Furthermore, it causes the creation of an intermediate node with a large capacitance. Of course, this means that the NOT gates drives the output of circuit through, for example, pass transistor or TG. Therefore, the short circuit power and, thus, the total power dissipation of this circuit are widely increased. Moreover, in the optimum PDP situation, the critical path delay will also be increased slightly. Therefore, to improve the XNOR circuit speed, the size of PMOS transistor (P5)and NOT gates should be increased.

2.4 PROPOSED XOR-XNOR CIRCUIT

The proposed structure of the simultaneous XOR–XNOR gate consisting of 12 transistors. The proposed XOR/XNOR and simultaneous XOR–XNOR structures were compared with basic XOR-XNOR circuit. The results indicate that the performance of the proposed XOR/XNOR and simultaneous XOR–XNOR structures is better than that of the compared structures. The proposed XOR and XNOR circuits have the lowest PDP and delay, respectively, compared with other XOR/XNOR circuits. Also, the delay of these proposed circuits is very close together that prevents the creation of glitch on the next stage. The proposed circuit for simultaneous XOR–XNOR has better efficiency in all three calculated parameters (delay, power dissipation, and PDP) when it is compared with other XOR–XNOR gates

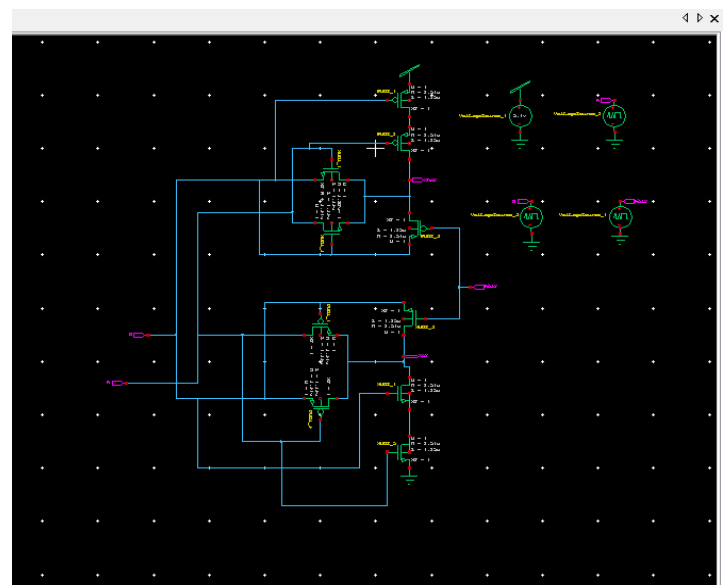


Fig-5:Proposed XOR-XNOR circuit

2.5 FULL ADDER CIRCUIT

Full adder is the adder which adds three inputs and produces two outputs. There are three types of basic structure on which full Adder is based static, dynamic and hybrid. Static full adders are less power consuming than dynamic and then more reliable. Dynamic full adder have faster switching speed, full swing voltage level and less number of transistors but suffer from charges haring, clock load, high power dissipation due to high switching activity and complexity. Hybrid full adder is basically the combination of static and dynamic full adder.

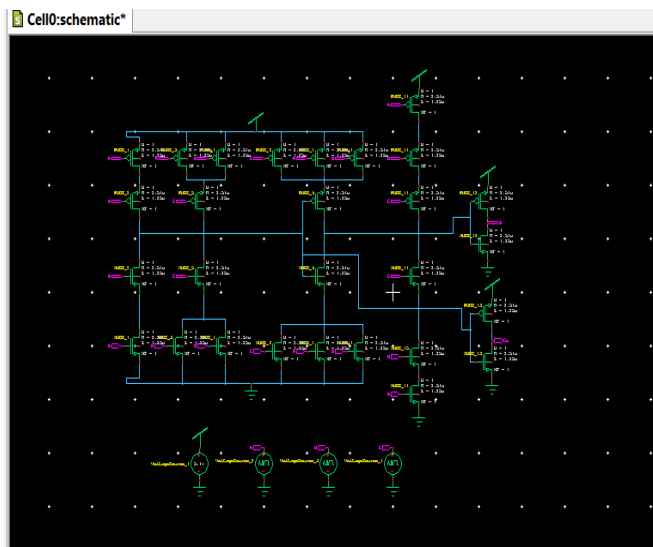


Fig-7 :Conventional CMOS Full adder

that of conventional CMOS full adder due to the reduction in the number of transistors. To produce the output Sum signal C and C compliment signals are used. The XOR, XNOR signals will be connected to the data select lines of 2-1-MUX. Due to the less capacitance of XOR and XNOR nodes the power consumption and delay of HFA 19T is less.

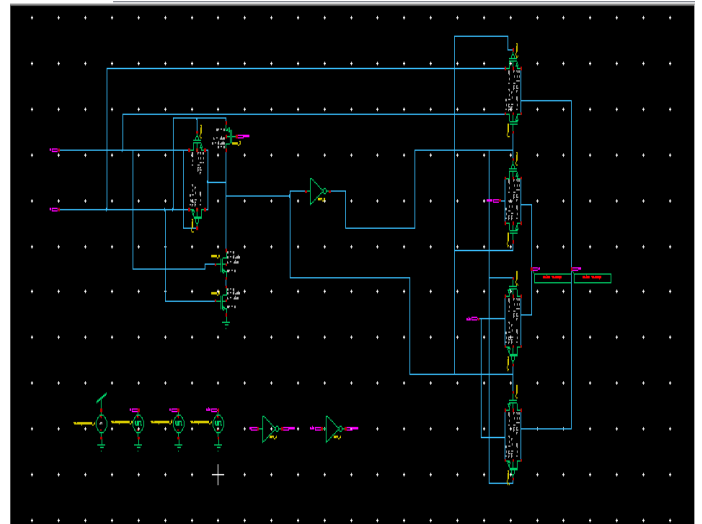


Fig-8 : Proposed Full Adder Circuit

3 RESULT AND ANALYSIS

The Tanner EDA tools were used to simulate the circuits. They offer complete design environment supporting analog/mixed-signal IC, MEMS and photonic design in highly integrated, end to end flow with an intuitive user interface for a quick learning curve and a low total cost of ownership through minimal IT support costs and competitive software license and maintenance costs.

3.1 WAVEFORM

Figure-9 depicts the obtained waveform of CMOS Inverter circuit

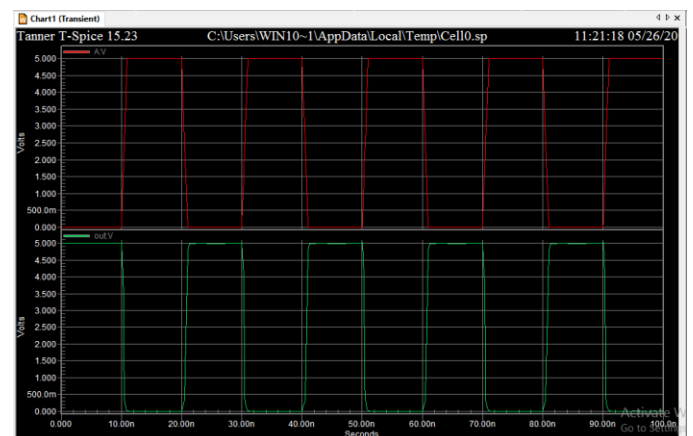


Fig-9: CMOS Inverter

2.6 PROPOSED FULL ADDER CIRCUIT

The new FA has been employed using switch hybrid logic style, and its designed by using the proposed XOR/XNOR circuit. The well-known four-transistor 2-1-MUX structure is used to implement the proposed hybrid FA cells. This 2-1-MUX is created with TG logic style that has no static and short-circuit power dissipation.

One way to reduce the power consumption of the FA structures is to use a XOR/XNOR gate and a NOT gates to generate the other XOR or XNOR signal. using the buffer on the output of a circuit is almost mandatory, especially in applications that the output capacitance of each stage is high. In practice, the driving capability of VLSI circuits is degraded due to the creation of the parasitic capacitors and resistors during the fabrication, as well as increasing the threshold voltage of transistors over the time, but the output buffer improves this situation.

The proposed HFA-19T is made by 19 transistors. The power consumption of proposed circuit is less than

Figure-10 depicts the obtained waveform of CMOS Half Adder.

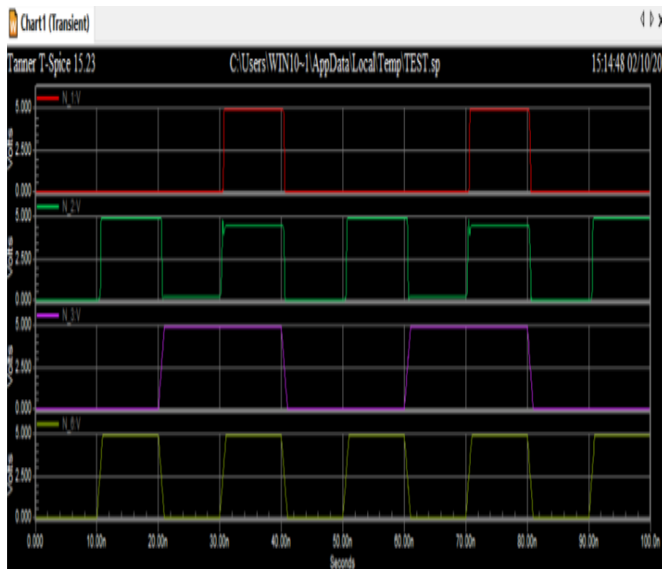


Fig-10: CMOS half adder

Figure-11 depicts the obtained waveform of XOR-XNOR Circuit.

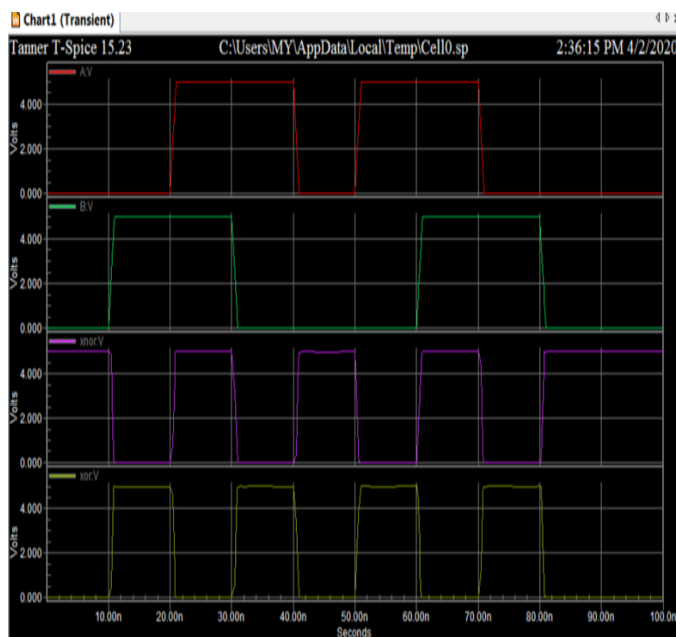


Fig-11: XOR XNOR Circuit

Figure-12 depicts the obtained waveform of proposed XOR-XNOR circuit

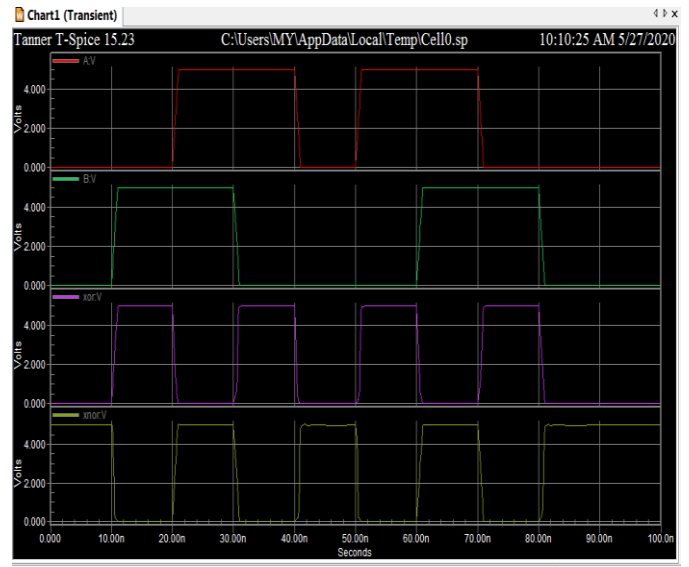


Fig-12: Proposed XOR-XNOR circuit.

Figure-13 depicts the obtained waveform of CMOS Full Adder

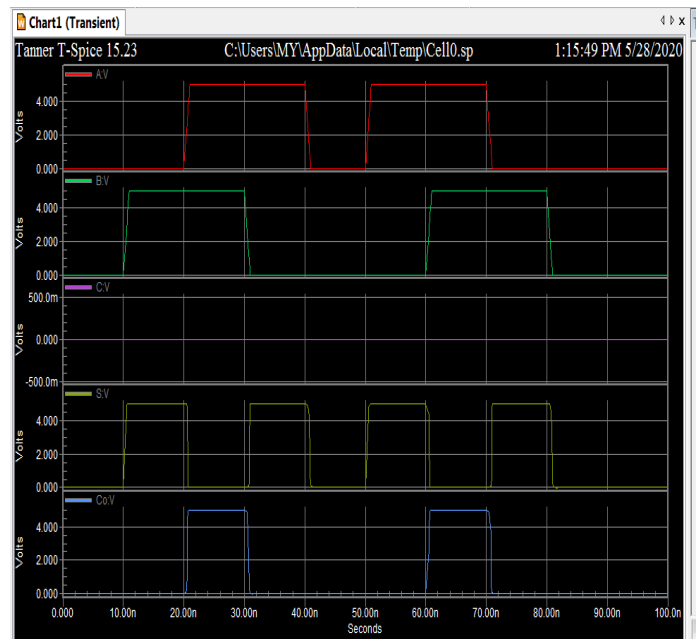


Fig-13: CMOS Full adder Circuit

Figure-14 depicts the obtained waveform of Proposed Full Adder Circuit

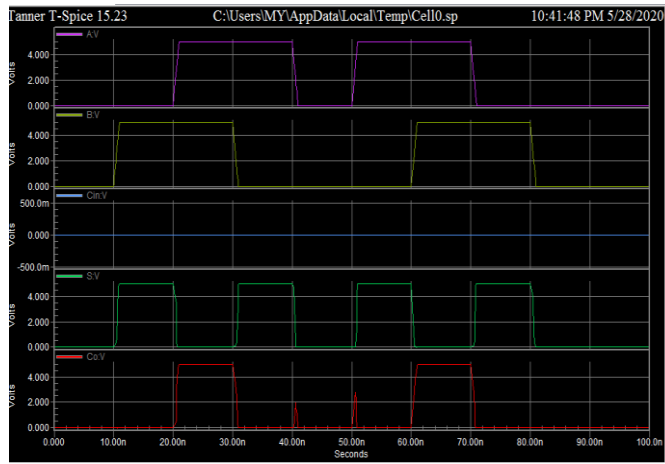


Fig-14: Proposed Full adder Circuit

3.2 COMPARISON OF POWER AND DELAY

As far as electronic circuits are concerned, power consumption is a major bottleneck of system performance. The main source is the leakage power consumption, so the power is reduced by using XOR-XNOR topologies.

Table -1: Comparison of power and delay table

CIRCUIT	POWER (W)	DELAY
Inverter	7.124e-006	9.5701n
Half Adder	5.082e-004	10.3n
XOR-XNOR Circuit	5.957e-004	39.989n
Proposed XOR-XNOR Circuit	9.364e-005	10.409n
Conventional CMOS Full Adder	4.479e-004	39.986n
Proposed Full Adder - HFA 19T	2.009e-004	9.994n

4 CONCLUSION

This paper proposes various logic circuits with XOR-XNOR technique, which resulted in better terms of power consumption. Simulations are carried out and the power analysis has been performed. From the observation it is evident that the circuit with proposed XOR-XNOR is the efficient design with minimum power consumption. Hence the proposed architecture is well suited for modern high performance designs where power dissipation is the major concern.

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