

Nine Level Active Neutral Point Clamped (9L-ANPC) Inverter with Reduced Power Switches and DC-Link Voltage

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Abstract - This paper presents novel architecture of Nine level active neutral point clamped (9L-ANPC) inverter topology for medium-voltage high-power application using 8 active switches and 2 flying capacitor to minimize total harmonic Distortion. This unique arrangement of 9L-ANPC uses reduced number of passive and active components. DC link voltage is controlled by PWM technique. This 9L-ANPC configuration has reduced number of power switches & requirement of DC link voltage is 50%. The simulation of 9L-ANPC is carried out in MATLAB - Simulink. Results indicate nearly a sinusoidal voltage waveform with less Total Harmonic Distortion (THD) of 1.70%.

Key Words: Multi-level inverter (MLI), Active neutral point clamped inverter (ANPC), THD, Neutral point clamped converter (NPC), Flying Capacitor (FC) inverter.

1. INTRODUCTION

Presence of Harmonics in output sine waveform are major problem in power converter. In medium and small industrial applications, square waveform are used. Whereas ideal sinusoidal are preferred for large applications in industries but it is problematic to achieve less distorted sinusoidal wave due to presence of THD, it resembles as major problem in converter, these harmonics effects in overall efficiency of the system by drawing more current and heating of conductor results in failure of insulation and maintaining cost increases. Hence harmonics has to be reduced in sine wave as much as possible. Multilevel Inverter helps to overcome voltage limiting ability of semiconductor devises. MLI were introduced in late 1975 advancement in semiconductor helps in maintaining good power quality with reduced switching losses, yet there are still novel technologies coming up to discover in emerging zones of application which makes MLI,s more attractive[1]-[3].

These inverters proposals several advantages than Two-level converters (2L)which generate AC source with input of DC source generating 2 voltage levels $+V_{dc}$ & -V_{dc} across load with harmonics in output waveform. Classic multi-level inverter (MLI's) topologies includes flying capacitor inverter (FC), Neutral point clamped inverter (NPC) and CHB inverters are different types of MLI. Phase leg of 3L-NPC is easy to control with simple PWM technique, but it has unequal loss distribution between the semiconductors and difficulty of capacitor voltage balancing considered as major drawback [4]. Number of switches required in NPC is less but balancing of capacitor is a major problem [5] However Flying capacitor balances the load & distribute losses equally but controlling is difficult due to its increased number of capacitors [6]. New FCMI structure makes full DC input available by using low frequency two switches & generates double RMS which helps to increase amount of output but number of power switches used is more and THD is about 6.26% [7]. Author has combined 5 level ANPC inverter and HBBB to form nine level ANPC to obtain better quality of voltage and current waveform, advanced method of controlling is required and implementation is complicated[8]. In neutral point clamped T-type inverter a nine step voltage waveform are generated but the number of components used is more [9]. In this paper a seven level output voltage is generated using 8 power switches which uses PWM to control but THD is 2.7% [10]

1.1 Demerits of conventional system

- There is a controlling complexity in flying capacitor inverter.
- Increases in switching loss and switching frequency in FC multilevel inverter.
- As level increases stage capacity also increases.
- For power conversion separate DC source are utilized in cascade inverter.

1.2 Merits of proposed system:

- Use of less active and passive elements.
- It has 4 capacitor with single DC sours as input.
- Easier and better control.
- Reduced number of component helps in improving system efficiency and reliability.
- Overall cost is less as compared to FC inverts and NPC inverters

2. Methodology

2.1 Analysis of proposed Topology

The typical MLI has come up with many problems when raising the level with THD. The NPC Multi-Level inverter becomes more complex as number of diodes increase with increasing output voltage steps, Flying Capacitor (FC) Multi-level inverter becomes expensive and heavy as requirement of capacitors increases.in case of Cascade-Multi-level inverter it requires variable voltage sources with increased voltage levels where as 9L-ANPC has only 8 switches hence switching losses is low & THD is reduced as output voltage level increases.

2.2 Block Diagram of 9L-ANPC using eight switches

The novel nine level ANPC multilevel inverter consists of 8 power switches & 4 capacitors 2 of them are DC link capacitor and 2 are flying capacitor, this circuit is connected to grid as shown in Fig. 1.

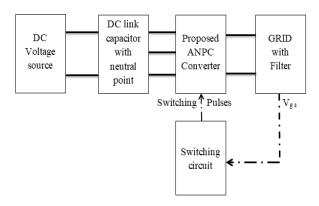


Fig. 1. Block diagram of 9L-ANPC

In this the voltage measured from grid and theta is extracted from the grid voltage and based on the theta extracted, the modulation sine wave signal was generated so that the inverter voltage will be in phase to grid voltage.

2.3 Features of proposed novel 8 switch 9L-ANPC converter

- Lesser number of active and passive components compare to other converters (FC, NPC etc.)
- Compared to conventional NPC, Cascade inverter and FC Inverter Families there is complete utilization of DC link Voltage.
- Voltage pressure on the switches is similar to the traditional inverter families such as NPC, Cascade inverter and Flying capacitor MLI, and individually power switch has a max voltage pressure of V_{dc} = $V_{DC}/2$
- Size and ESR is reduced because DC-link capacitor voltage stress is about half.

3. Circuit Design & Description

9L-ANPC is a hybrid topology which combines inverter families of NPC, FC or Cascade H bridge multilevel inverter, all these methods uses more number of components which in turn increases total cost of the converter. This proposed topology designed with minimum number of switches.

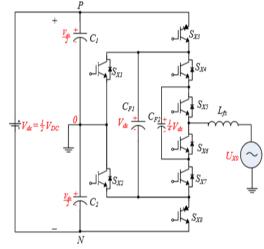


Fig. 2. Circuit Diagram of 9L-ANPC

The novel active neutral point clamped MLI of 9 level circuit is designed with four capacitors C_1, C_2, C_{F1} and C_{F2} and eight power switches namely $S_{x1}, S_{x2}, S_{x3}, \dots, S_{x8}$ (where X is phase(R,Y,B)), switches used may be IGBT or MOSFET, Schematic of 9L-ANPC is shown in Fig.2 along with this switching signals circuits. In this eight switches S_{x3}, S_{x7} are Reverse blocking Insulated-Gate Bipolar Transistor (RB-IGBT) with series diode or it may be 2 MOSFETs with series Diode, and other switches $S_{x1}, S_{x2}, S_{x4}, S_{x5}, S_{x6}$ are unipolar voltage devises with reverse conducting path such as 6 IGBT's / 6

MOSFET', similar to 7L- ANPC [10], C_1 and C_2 are two series connected capacitors and their voltage is 1/2 of the DC link voltage and remaining six switches are S_{x1} , S_{X4} and S_{X5} or S_{X2} , S_{X6} , S_{X7} Routes, which attached to AC terminal to the dc-link mid-point "0" as DC neutral point. The Flying Capacitor C_{F1} is charged by S_{X3} and S_{X8} at each switching cycle from the input V_{dc} to form a full simulated dc-bus of 3^{rd} and 4^{th} level (0.5V_{dc} to 0.75V_{dc} to V_{dc} or $-0.5V_{dc}$ to $-0.75V_{dc}$ to $-V_{dc}$) voltage waveform at load side before the filter. Likewise, the charging of Flying Capacitor C_{F2} by S_{X3} , S_{X4} and S_{X6} in the positive cycle and negative cycle through S_{X5} , S_{X7} and S_{X8} to generate $1^{st}\,and\,2^{nd}\,levels$ (0 to $0.25V_{dc}\,or\,0$ to $-0.25V_{dc}$ & $0.25V_{dc}$ to $0.5V_{dc}$ or -0.25Vdc to $-0.5V_{dc}$). At ideal operation, the projected inverter has 9 output voltage levels: $\pm V_{dc}$, $\pm 3V_{dc}/4$, $\pm V_{dc}/2$, $\pm V_{dc}/4$, 0 in positive & negative cycle and as reprasentated in Fig.3 and dclink voltage1is defined as V_{dc} for the proposed 9L-ABNPC, and, where $V_{dc} = V_{DC} / 2$.

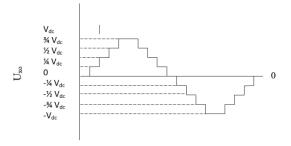


Fig. 3. Nine output voltage levels

3.1 Switching Operation of Nine level Active Neutral point clamped Inverter

Process of Active neutral point clamped inverter for power flow conversion from Direct current to Alternative current flow is explained using twelve Switching states as shown in Table-I which generates output of nine level voltage, using eight switches and four capacitor as detailed in circuit description. Each capacitor is maintained at DC link voltage of $\frac{1}{2}V_{dc}$ and voltage of Flying capacitor C_{F1} and C_{F2} is V_{dc} and 0.25V_{dc} respectively. Two switches S_{X1} and S_{X2} which are known as active switches are clamped to neutral point along with Capacitors $C_1 \& C_2$ for equal voltage sharing between switches S_{X3} - S_{X8} and helps to create switching states of Zero voltage.

The nine level ANPC inverter (9L-ANPC) switching table is shown in Table I:

Table I:	Switching	states	of 9L	-ANPC:
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State	Uxo	S _{x1}	S _{x2}	S _{x3}	S _{x4}	S _{x5}	S _{x6}	S _{x7}	S _{x8}
А	0	1	0	0	1	1	0	0	0
В	0	0	1	0	0	0	1	1	0
С	$1/4V_{DC}$	0	0	1	1	0	1	0	1
D	1/4V _{DC}	0	1	0	0	1	0	1	0
Е	1/2V _{DC}	0	0	1	1	1	0	0	0
F	3/4V _{DC}	0	1	0	1	0	1	0	0
G	Vdc	0	1	0	1	1	0	0	0
Н	-1/4VDC	0	0	1	0	1	0	1	1
Ι	-1/4VDC	1	0	0	1	0	1	0	0
J	-1/2V _{DC}	0	0	1	0	0	1	1	1
К	-3/4V _{DC}	1	0	0	0	1	0	1	0
L	-VDC	1	0	0	0	0	1	1	0

The PWM technique is used for the proposed 9L-ANPC inverter which uses all 12 switching states to produce the appropriate voltage level at inverter output as shown in Fig.4 and compared with single modulation V_{ref} voltage with 4 carrier wave for positive cycle & remaining 4 carrier waves for negative cycle CR1, CR2, CR3, CR4 and -CR1, -CR2, -CR3, -CR4 respectively.

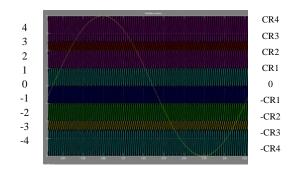


Fig. 4. The pulse width modulation (PWM) for 9L-ANPC

4. SIMULATION RESULT

Operation of 9L-ANPC is performed using MATLAB-SIMULINK by taking a component parameters as shown in Table-II. 9L-ANPC is simulated as shown in Fig.5 with input of 400V DC supply to get output voltage of 230V which is filtered to obtain nearly sinusoidal wave of 230V V_{ph} and current of 10A at load for both R and RL load.

Table II: Components and parameters used forSimulation

Parameters	Value				
Input voltage(V _{dc})	400V				
Output voltage (V _{ac})	230V				
Power rating(P _o)	2.2 kVA				
Dc-link capacitor ($C_1 \& C_2$)	10 mF,200V				
Flying capacitor (C _{FC1})	10 mF,400V				
Flying capacitor (C_{FC2})	10 mF,100V				
Carrier frequency (f _s)	5 kHz				
Line frequency(f)	50 Hz				
Load (RL)	20Ω and 200mH				

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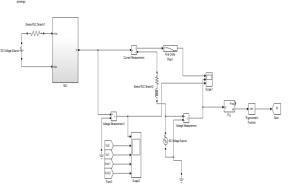


Fig.5. 9L-ANPC in Mat lab

The proposed converter consists of 8 switches and two flying capacitors and two input capacitors with neutral midpoint. The pulses will be provided with the help of switching circuit based on the switching Table II.

The switching pulses for eight switches nine level inverter is shown in Fig.6:

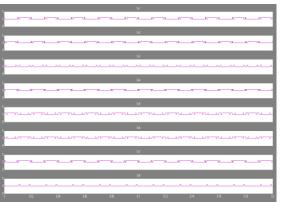


Fig.6. Switching pulses for 8 switch

Fig.7 represents the output voltage level & capacitor voltage waveforms of 9L-ANPC

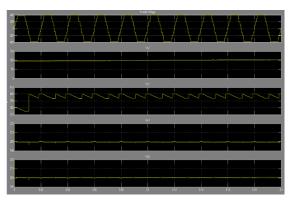


Fig. 7. Capacitor C_{F1} & C_{F2} waveforms of 9L-ANPC for RL load

The output of grid voltage, Grid current waveforms and 9 steps of 9L-ANPC for RL load are shown below in Fig.8.

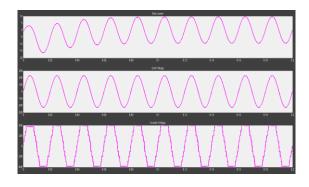


Fig.8. Voltage & Current Output of 9L-ANPC for RL load

The Total harmonic distortion for RL load is shown below in Fig.9:



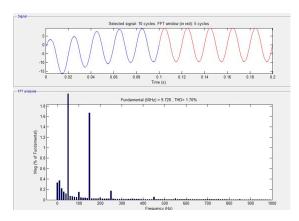


Fig. 9. THD of 9L-ANPC

Total harmonic distortion of proposed 9L-ANPC for RL load is 1.70% which is less than 7L-ANPC inverter with THD of 2.4% [10].

The grid voltage, current waveforms and 9 steps of 9L-ANPC for R load is shown in Fig.10 following graphs:

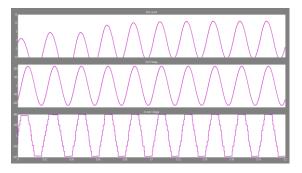


Fig. 10. Voltage & Current Output of 9L-ANPC for R load

The Total harmonic distortion (THD) for R load is shown in Fig.11:

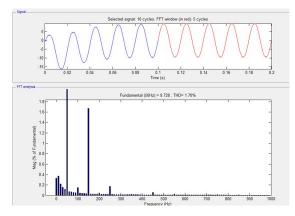


Fig. 11. THD of 9L-ANPC

Total harmonic distortion of proposed 9L-ANPC inverter for R load is 1.70%. THD for both R and RL load is same.

5. CONCLUSION

In this paper a new nine level active neutral point clamped (9L-ANPC) inverter is proposed with analysis of THD using only 8 power switches for single phase (230V) with reduced Dc-link voltage to generate sinusoidal wave of 1.70% THD at load side, which improves over-all efficiency of the system and reduces the total cost of the inverter due to reduced number of power switches.

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