

# FPGA IMPLEMENTATION OF A DECISION TREE CLASSIFIER USING DEEP LEARNING ALGORITHM

Lakshmipriya R<sup>1</sup>, Anita Titus<sup>2</sup>

<sup>1</sup>Student, Department of Electronics and Communication Engineering, Jeppiaar Engineering College, Chennai, India

<sup>2</sup>Head and Professor, Department of Electronics and Communication Engineering, Jeppiaar Engineering College, Chennai, India

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**Abstract** – Current technology evolution is closely associated with the success of deep learning. Conventional classification systems rely on data representation by feature engineering, a time-consuming process that requires expert knowledge for feature extraction. Alternatively, deep learning does not require a domain expert for feature extraction and organization of the data. In this project, preliminary experiments using a deep learning approach is employed to classify normal and diseased human lung CT images based on a decision rule. A method based on the metric score calculation for training the algorithm and the comparison of these metric scores for final classification is proposed. The implementation of the classifier is brought about in VHDL using Xilinx ISE design Suite 14.1 version. The proposed architecture is implemented by fitting all trained network parameters on-chip using MATLAB R2017a and Xilinx ISE design suite 14.1 targeting EDGE XC7A35T Artix 7 FPGA device. Power analysis of the proposed classifier architecture showed 45% reduction in power consumption compared to existing architectures. Accuracy of the proposed algorithm was found to be around 98%. The proposed architecture results in less computational complexity when deployed in hardware.

**Keywords:** Deep learning, classification, image processing, FPGA, VHDL

## 1. INTRODUCTION

Deep learning and machine learning approaches are employed to train a computer system for prediction and decision making. Machine learning and deep learning enables extraction of patterns and their automatic reasoning by providing intelligence to the computers. Machine learning provides computers with the ability to learn without intensive programming, whereas deep learning allows the system to read and understand the data [1,2]. Deep learning majorly employs neural networks for data prediction, where deep graph containing numerous processing layers of linear and nonlinear conversions is used [3].

Medical image processing is a significantly growing research area due to its impact in timely detection and treatment of diseases. Image processing comprises the

concepts of pattern recognition, object detection, reasoning and classification etc., allowing pattern extraction with high accuracy from a specific data. Employing a simple mathematical model will not accurately differentiate lesions and organs in image processing, while machine learning algorithms applies pixel-based assessment of the images and can be effectively applied for studying specific diseases. Machine and deep learning methods classifies multi-dimensional medical data based on automatic decision-making [4,5].

Decision tree is one of the easiest classification algorithms belonging to the supervised learning algorithm family. Decision tree algorithm can be employed for solving regression and classification problems. It creates a training model that can be used to predict the class of a target variable by applying simple decision rules acquired from prior trained data. Decision tree structures are majorly adapted to organize classification, to find out the steps that eventually leads to a class. Decision trees starts with root nodes from which the tree grows and evaluating each attribute using an algorithm a path for tree growth is found. Decision making is based on if else statements and this process repeats till the leaf node is reached [6].

Structural and functional information about various human organs can be obtained in Computer Tomography (CT) scan imaging using X-ray. Based on the X-ray absorption profile; the fact that different tissues absorb X-rays differently, they are used in diagnosis producing a reconstructed CT image. In a CT image bones appear white and soft tissues appear grey. Lung cavities filled with air appear black. CT is a supplement to magnetic resonance imaging and ultrasonography. CT imaging is used in diagnosis of liver, chest, brain, abdomen, spine and pelvis.

FPGAs belong to class of programmable logic devices (PLD) providing benefits of integrated circuits with reconfigurable flexibility of GPPs. FPGAs implement sequential logic using flip-flops (FF) and combinational logic using look-up tables (LUT). Modern FPGAs has components such as processor cores, arithmetic and communication cores and a RAM. Currently FPGA trends are moving towards system-on-chip design approach [7].

They are effectively replacing Application specific integrated circuits (ASICs) and application specific standard products (ASSP) for fixed function logic. The most popular languages for FPGAs have been Verilog and VHDL, both examples of hardware description languages (HDL).

## 2. LITERATURE REVIEW

Numerous research groups have reviewed and reported the emerging trends of deep learning applications in medical image processing [8,9]. Convolutional neural networks are replaced by deep learning algorithms as they are limited by the difficulties in computational implementation such as high memory bandwidth requirement and intensive computation resources. A deep CNN (SqueezeNet) for image classification enabling significant reduction in the networks' model size and improvement in the accuracy and performance was proposed Hailesellase et al., 2018 [10]. A supervised learning approach for lung cancer CT-scan image classification was proposed by Ahmed et al., 2019 [11]. A classical SVM classifier was combined with supervised learning algorithm for classification and detection of lung nodules enabling early diagnosis of lung cancer.

Sasireka and Santhosh 2019 [12] proposed a decision tree-based label feature classifier (DTLFC) mechanism. A VLSI implementation of flexible architecture for Decision Tree classification in data mining using c4.5 algorithm using Xilinx 13.2 version with device XC5VLX110T was proposed by Davis and Immanuel 2013 [6]. Chien and Pottie 2012 [13] proposed a universal hybrid decision tree classifier. The proposed tree classifier was able to flexibly implement different decision rules at its internal nodes. Similarly, Narayanan *et al.*, 2007 [14] has proposed a hardware implementation of decision tree classification algorithm. The architecture was implemented on a Xilinx ML310 board using the Xilinx XPS 8.1i and ISE 8.1i software, the architecture yields 5.58X speedup.

## 3. METHODOLOGY

Various processing steps are performed on the input medical images before the detection and classification the of output as elaborated in figure 1. Firstly, input medical images to the deep learning algorithms are pre-processed for the removal of distortion and noise. The images are then divided into different segments to zoom the interested area (ROI). Features are then extracted from the segments through informal retrieval techniques. Desired features are selected removing the noise. A database is created based on the feature parameter metric scores. Two processes are involved before final classification; training (learning) and test phase. In the training phase, the network is pre-trained by providing 80% of the input data (training data) using supervised learning method. In test phase remaining untrained images are given as input to the DT classifier,

where the test input features are compared with the pre-trained image registry in the database for metric score matching. Finally, the classifier is used to classify the extracted data and make predictions based on this classification. These steps are used in every experiment of machine learning.

A VHDL code based on behavioural modelling was developed and implemented onto an EDGE ARTIX-7 FPGA development board. The hardware consists of EDGE ARTIX-7 board and an Arduino UNO LCD driver. The FPGA acts as a master control and decision-making architecture & it gets and gives the control codes. The FPGA controls the input comparative bits through continuously running counter module in the hardware. FPGA compares the result and produces the master control word at the output LCD. The ARDUINO UNO is used as an LCD driver and communicating agent with FPGA. Once the results are tested, they are displayed in LCD display as disease names. Level converter is used to equalize voltage levels of FPGA and ARDUINO. The hardware block diagram is represented in figure 2.

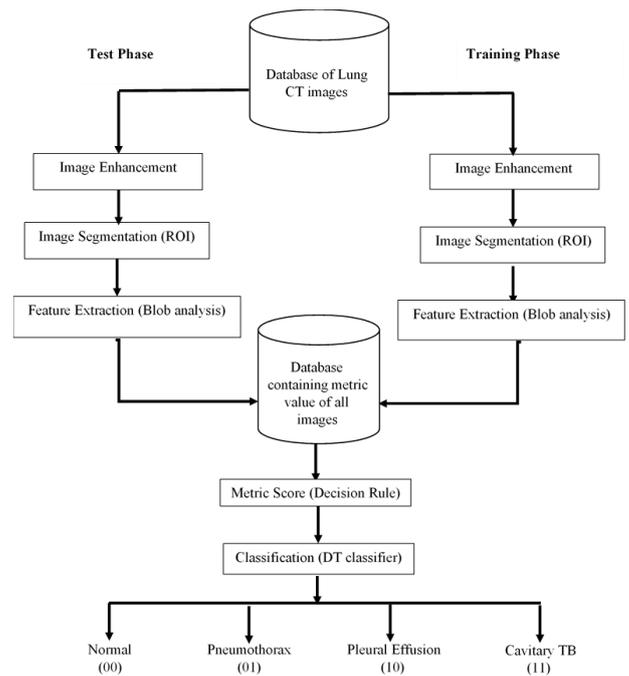


Fig – 1 Block diagram of the proposed system

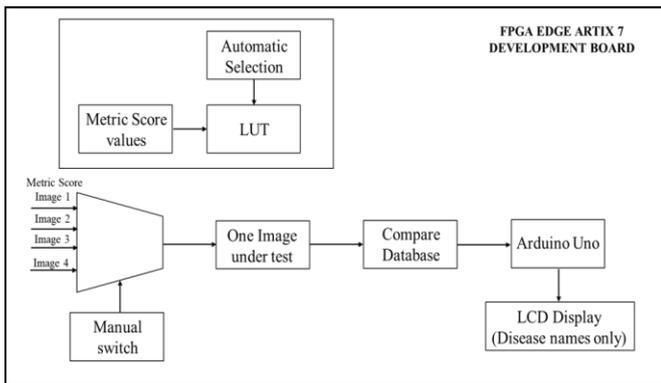


Fig – 2 Hardware architecture block diagram

## 4. RESULTS AND DISCUSSIONS

### 4.1. Pre-processing

Human Lung CT scan images were given as inputs to the deep learning algorithm. The MATLAB software is used for pre-processing purposes. Pre-processing is the process of image improvement by suppressing unwilling distortions or enhancing some important features for further processing.

Image enhancement involves the process of improving quality and information content of the original image before processing. Enhances the image from corruption or interference and noise. Image enhancement was carried out using Gabor filter technique. The enhancement percentage was found to be 57.1%.

Image is partitioned into meaningful segments having similar features and properties using image segmentation technique. Watershed and Region-based segmentation techniques were applied and based on the discontinuities and similarities the image was segmented to obtain the region of interest (ROI).

Feature extraction involves reducing the number of resources required to describe a large set of data. Three techniques were employed for feature extraction: Binarization, Blob analysis and Mask approach. Binarization transforms data features of any entity into vectors of binary numbers. Blob analysis is a basic method of image processing for analyzing shape features, such as presence, number, area, position, length and direction of lumps of an object. Masking is traditionally used for extraction of texture features to arrive at a detailed view of the ROI. It filters images with five types of masks, namely level, edge, spot, ripple, and wave. A feature weight vector and a masking or selection vector from the ROI are calculated in the process. Feature weights are real-valued, whereas the mask values are either 0 or 1. Each feature is multiplied by both its weight value and its mask value prior to classification to obtain the target mask i.e, metric score. A feature set table is formed from the extracted features.

### 4.2. Classification

Classification in machine learning involves two steps, learning and prediction step. Learning step involves development of a model based on given training data. Prediction step involves predicting the response of the given data using the developed model.

The feature extracted results of the training and test phases are compared with the help of the feature set formed. Based on the Metric score and labeling, the images are classified to their respective classes. Supervisory learning for classification and Decision Tree (DT) as the classifier is employed in this project.

The decision tree classifier uses supervisory learning method. The classification is carried out in two major steps. They are learning or training step and prediction step. The DT classifier works based on an attribute selection measure or a decision rule. The DT classifier uses a tree structure for classification problems. The tree structure has three nodes namely root node, decision node and leaf node. The learning step is considered as the root node, which contains all the training inputs metric score (dataset) obtained during the training phase of the classifier. The root node splits the dataset into subsets. Each subset contains a decision node with one or two branches, which uses ‘if else’ statement to find a desired attribute using top-down traversal method. Here in the proposed DT classifier, desired attribute is the metric score match between the test and training inputs. Once the desired attribute is found, the search stops and the leaf node contain the predicted result of the classification problem. The predicted result shows the classifier output [6,12].

### 4.3. Hardware Implementation

The proposed low power VLSI classifier architecture contains a LUT, Metric score database and an automatic selector which altogether forms the reconfigurable RAM part of the architecture. The input images are given one by one separately. Using the manual switch, metric score of any one of the four-test image is given as input.

The metric score (decision rule) is the match between the test input sequence of pixels & the trained input sequence of pixels at 40Mhz sampling frequency. The metric score of the image under test is compared with metric score database in the FPGA RAM. The metric score database of the FPGA RAM contains all the trained inputs metric score obtained during the training phase.

Finally based on the metric score match of the test and training input, the image under test is predicted and classified to its respective class and the result is displayed using an Arduino driven LCD display.

The classifier code run on the hardware classifies the normal lung CT images from the diseased lung CT images; and it further classifies the diseased lung CT

images based on the extracted ROI from the iterated images. Figures 3, 4, 5, 6 shows the iterated images and classifier outputs of the classes normal with label 00, pneumothorax with label 01, pleural effusion with label 10 and cavitary TB with label 11 respectively, based on

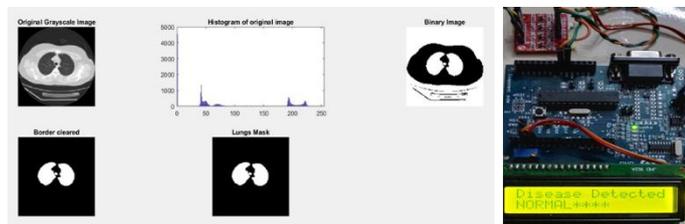


Fig – 3 Iterated images and classifier outputs of the class Normal

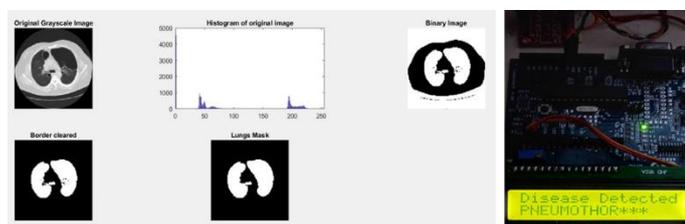


Fig – 4 Iterated images and classifier outputs of the class Pneumothorax

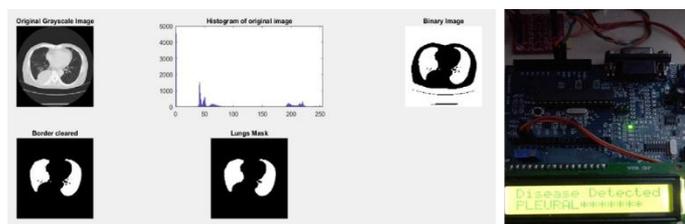


Fig – 5 Iterated images and classifier outputs of the class Pleural effusion

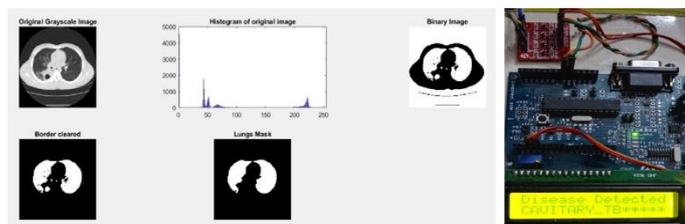


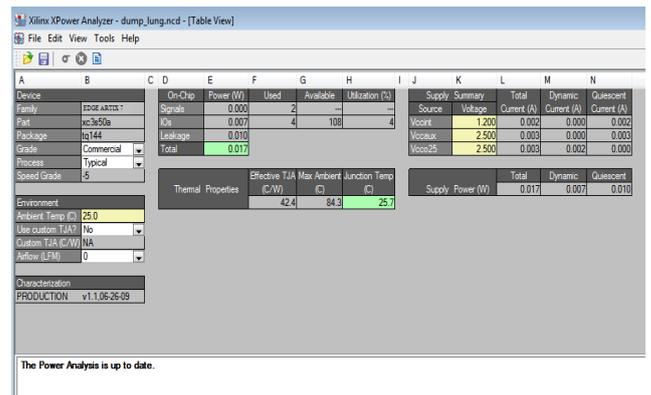
Fig – 6 Iterated images and classifier outputs of the class Cavitary TB

#### 4.4. Power analysis of the proposed architecture

The main aim of the proposed architecture is to reduce the over-all power of the classifier system by implementing low power principles. Using a single reconfigurable RAM for circulating the whole bunch of data within the architecture, efficiently reduces the power consumed for the process. A pipelined approach is proposed for efficient utilization of hardware processing cores. Power consumption in the proposed

the label and metric score of the input images given during the training phase using supervised learning. The outputs are obtained and displayed through the Arduino driven LCD display of the classifier hardware. Accuracy of the classifier was found to be 98%.

architecture is reduced to about 45% compared to existing architecture. Figure 7 shows the power analysis calculation of the classifier.



Device	On-Chip	Power (W)	Used	Available	Utilization (%)	Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Family	EDGE ARTIX7	Signals	0.000	2	--					
Part	xc3a50g	I/Os	0.007	4	106	4	Vccint	1.200	0.002	0.000
Package	qs144	Linkage	0.018				Vccaux	2.500	0.003	0.000
Grade	Commercial	Total	0.017				Vccp2s	2.500	0.003	0.002
Process	Typical									
Speed Grade	-S									
Thermal Properties		Effective TjA	Max Ambient	Junction Temp						
		(C/W)	(C)	(C)						
		42.4	84.3	25.7						
Supply Power (W)		Total	Dynamic	Quiescent						
		0.017	0.007	0.010						

Fig – 7 Power analysis- Calculation of power consumed by the classifier

#### 5. Conclusion

A deep learning algorithm was developed using Decision Tree model for classification of CT images of normal and diseased human lung. The decision tree working on attribute selection measure (decision rule) is able to function better with limited computational power achieving greater accuracy. The developed algorithm was implemented in VHDL using Xilinx ISE design Suite 14.1 version and checked for its overall power consumption and accuracy. The accuracy was found to be around 98%. 45% reduction in power consumption was observed. The code was implemented on an EDGE ARTIX-7 FPGA development board to obtain an efficient low power VLSI classifier architecture. The developed algorithm can be implemented for similar image processing applications with its high accuracy. FPGA implementation of the classifier model can be further improved by using a single BRAM and Look-Up Tables (LUTs) thereby achieving area reduction and power consumption reduction. The classifier architecture can be further tested for its specificity and sensitivity.

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