

Simulation and Performance Analysis of SEPIC(DC-DC) Converter using Genetic Algorithm based PI Controller

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Abstract - This paper proposes the simulation design and performance analysis of SEPIC (Single-Ended Primary Inductor Converter) by employing genetic algorithm tuned Proportional integral (PI) controller to observe Output voltage stability, Total Harmonic Distortion (THD), Power Factor (PF). SEPIC is widely used in battery operated or in battery charging unit for its relevant feature of step up and step down voltage without changing polarity. The performance analysis of the proposed converter in discontinuous conduction mode is framed for above mentioned methods using Matlab/simulink based. Result reveal that the GA-tuned PI controller gratifies performance to other converter in terms of Power Factor, percentage total harmonic distortion.

Key Words: SEPIC converter, Total Harmonic Distortion, PI Controller, Genetic algorithm, sliding mode controller.

1. INTRODUCTION

Now days we need to good fuel utilization and preventing the green house effect with minimization use of non renewable resources. Hence automotive industry is shifting to electrified vehicles also domestic power supply is created by using PV system. The recent and upcoming technology comprises an energy storage known as BES(battery energy storage), which charging incorporates certain power electronic interfacing circuit as illustrated in [1-2]. These power electronic circuits that regulate the charging voltage for BES should be designed efficient enough to maintain the input power quality indices as per the IEC 61000-3-2 standard [3]. However, conventional EV battery chargers are supplied from an AC source using filtered using filtered output of a diode bridge rectifier. This is produces the non-sinusoidal line current and it cause line current with a lot of harmonic. This pulsating or non-sinusoidal current reduces the power factor and efficiency. Hence it necessitates to developing the power factor correction (PFC) circuits. To improve the efficiency, power factor near to unity and minimize the THD. For PFC several types of passive and active PFC schemes have been exists. In that passive PFC circuits are not relevant due to its bulkier and expensive. In an active PFC circuit, DC-DC converters can be made to emulate as a resistor on supply side by operating at a high switching frequency. The implementations of different PFC schemes have been proposed by several researchers. A buck converter based

PFC was described in [4-5] and it has an advantage of low ripples in the output voltage. The disadvantages are (i) output voltage is always lesser than the input voltage; (ii) no isolation can be provided between the power and control circuit; (iii) requirement of a filter at the input side. PFC circuit using a boost converter is proposed in [6-7]. Boost convert has advantage of elimination of a filter at the input side; limitation of the boost converter and buck converter is cannot be performed step up and step down voltage using one particular circuit. Hence buck-boost based PFC scheme is given in [8-9]. This scheme have major demerits is required filter at input side and get inverted output voltage and this same results we get from cuk converter which has been proposed in [10]. To overcome the demerits of the above mentioned DC-DC converter, a DC-DC single ended primary inductance converter (SEPIC) is chosen for PFC in this scheme. The SEPIC has become most prominent topologies, which has the features of continuous input and output current due to the input output inductors. This property makes it more relevant for PFC application [9-11]. It has high power density and fast transient response compare to other. Also one more advantage is it can be operate as buck as well as boost mode. Due to coupling capacitor its provided isolation between source and controller side. It has given output voltage without polarity inversion with good steady state performance. But SEPIC has two inductor and two capacitor hence it become fourth order system and it become more complexity and increases the computational time. To reduce this two critic point SEPIC fourth order system can be converted into second order using pade approximation method [12]. A PI controller is widely used in power converter because of the robust performance with wide range of operation condition and alleviation of implementation. Here the PI controller is initially tuned with the Z-N technique [13-14]. The PI controller parameters are then tuned by an efficient optimisation technique like genetic algorithm (GA) [15-16]. Therefore, it is proposed to implement the closed loop control of DC-DC SEPIC PFC scheme using the Genetic algorithm PI controller.

The paper is organised as follows. Section2 clarify the modelling and design of the DC-DC SEPIC. Section 3 explains the simulation and result of SEPIC based PFC scheme. Section 4 describes the genetic algorithm tuning methods. Section 5 explains the analysis study of SEPIC

using Matlab FFT analysis tool. Section 6 concludes the proposed work from the comparative result.

2. Modelling and design of the DC-DC SEPIC

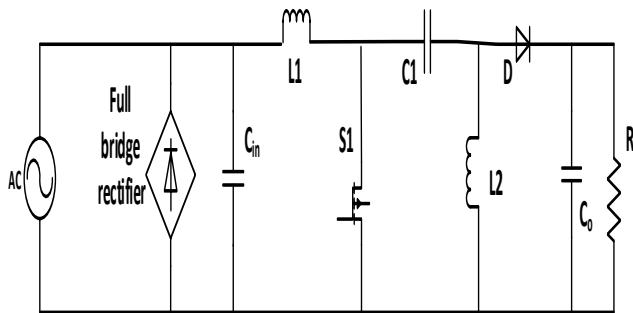


Fig-1: SEPIC Converter

The circuit diagram of the DC-DC SEPIC is shown in fig-1. SEPIC converter swaps the energy between the capacitors and inductors in order to convert from one voltage to another and it is controlled by switch S1, which is typically transistor family such as a MOSFET.

2.1 Operation modes of SEPIC

The converter operation can be divided into two modes which are depending on switch ON and switch OFF condition [17].

2.1.1 When switch is ON mode:

In this mode switch S1 is on and current in inductor increases linearly and approximate voltage across the inductor is equal to input voltage it is shown by green line in Fig-2. Coupling capacitor C1 convey energy to the load by boost the magnitude current i_{L2} and thus increase the energy storage in L_2 . Load current I_L is supplied by C_o .

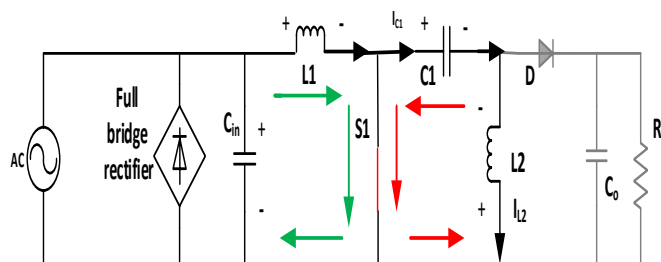


Fig-2 SEPIC when switch is on mode

After referring Kirchoff's voltage and current law the following equation obtained.

$$L_1 \frac{di_{L1}}{dt} = V_{in} \tag{1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{C1} \tag{2}$$

$$C_1 \frac{dV_{C1}}{dt} = -i_{L2} \tag{3}$$

$$C_o \frac{dV_o}{dt} = -\frac{V_{C_o}}{R} \tag{4}$$

2.1.2 When switch is OFF mode:

In this mode switch S1 is OFF then power delivered to the load by both Inductor L_1 and L_2 . During this off cycle C1 is charged by inductor L_1 and C2 is charged by inductor L_1 and L_2 . As in shown in fig-3

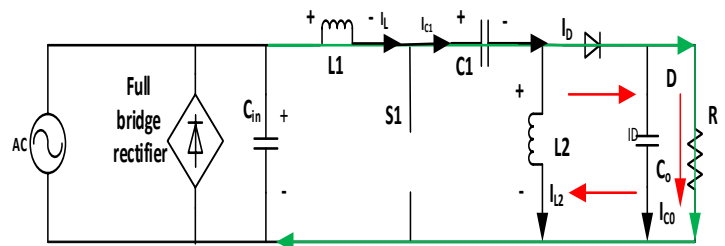


Fig-3 SEPIC when switch is OFF mode

After referring Kirchoff's voltage and current law the following equation obtained.

$$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{C1} - V_{C_o} \tag{5}$$

$$L_2 \frac{di_{L2}}{dt} = -V_{C1} \tag{6}$$

$$C_1 \frac{dV_{C1}}{dt} = i_{L1} \tag{7}$$

$$C_o \frac{dV_o}{dt} = i_{L2} + i_{L2} - \frac{V_{C_o}}{R} \tag{8}$$

The state variables of SEPIC are i_{L1} and i_{L2} , and the voltages V_{C1} and V_{C2} . From the above equations (1 to 8) of ON and OFF operation of a switch, using average the state space average technique [20] SEPIC can be written as follows

$$\frac{d}{dt} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} \frac{V_{C1} + V_{C2} - 2V_{in}}{L_1} \\ \frac{V_{C1} + V_{C2}}{L_2} \\ -\frac{i_{L1} - i_{L2}}{C_1} \\ -\frac{i_{L1} - i_{L2}}{C_2} \end{bmatrix} \gamma + \begin{bmatrix} 1 \\ L_1 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{9}$$

$$\dot{X} = AX + B\gamma + C \tag{10}$$

where γ is the status of the switch and X are the state variables of currents i_{L1} and i_{L2} , voltages V_{C1} and V_{C2} and

their derivatives respectively γ is 1 when the switch is ON and γ is when switch is OFF.

2.2 Design of SEPIC parameter:

DC-DC SEPIC parameters are designed by using the following specifications [18-20]: switching frequency: 10KHz, input voltage 24V, load resistance R_L : 50 ohm, Duty cycle: 0.68; $I_0=1A$

S.no	Parameter	Value
1	Inductor $L1=L2$	0.47mH
2	Coupling Capacitor	200 μ F
3	Output Capacitor	1000 μ F
4	Load resistance	50 ohm
5	Switching frequency	10KHz

Table-1 The parameter value for simulation

The calculated parameter values from above table are substituted in the equivalent state space model defined in (10). Then we get fourth order system of SEPIC in the input output relationship.

$$\frac{V_{out}}{V_{in}}(s) = \frac{1.6 \times 10^{-6} s^2 + 3.4816}{2.5 \times 10^{-12} s^4 + 5.12 \times 10^{-11} s^3 + 2.05842 \times 10^{-5} s^2 + 2.82 \times 10^{-4} s + 5.12} * V_{in} \tag{13}$$

3. Simulation and Result of SEPIC

The input AC voltage is converted in DC voltage by using the DBR. The output voltage of DBR is fed to SEPIC as a input. To controller the output PI controller is used. The resultant voltage is given to the PI controller. PI Controller calculates an error value as the difference between a measured process variable and a desired set point. The controller attempts to minimize the error by controlling the process through the manipulated variable. Manipulated variable is

$$MV(t) = K_p * e(t) + K_i \int e(t) dt \tag{12}$$

The simulation is done in MATLAB simulink.

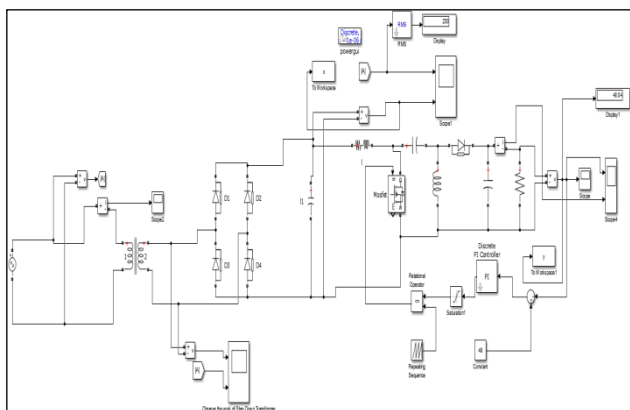


Fig-4 Simulation diagram of SEPIC using PI controller

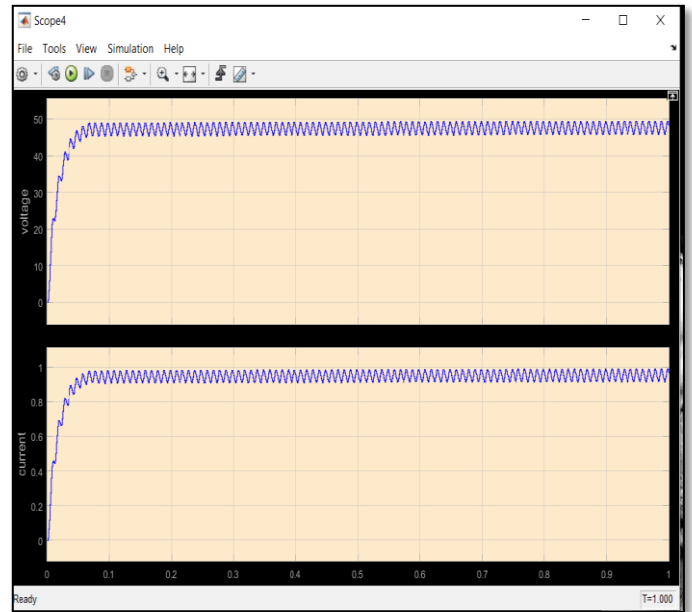


Fig-5 Simulation result of SEPIC using PI controller

Shows the output voltage when $V_{ref} = 48$ and output current of SEPIC under start-up when applied input voltage. It can found that the converter output voltage and output current have negligible overshoot with settling time of 0.1s.

4 Genetic Algorithm

PI controller is tuned using GA. GA is one of the optimisation method and it is based on natural evolution. It is uses for searching technique to find approximate solution for optimisation. It gives set of the solution which is maximising the fitness function. The fitness function is determined by applying one of the performance criteria integral time absolute error (ITAE).

$$ITAE = \int |e(t)| dt. \tag{13}$$

Fig-6 is steps involved in the GA optimisation process

This fitness function is then optimized by the GA such that the voltage and current errors and also harmonic contents get reduced with the optimized K_p and K_i values. Therefore, PF will be higher with less %THD. This calculation is realized for all the individuals of the population of GA. The optimum values of PI controller parameters determined by the GA for both voltage and current controllers are found to be $K_p = 0.1$, $K_i = 1$. With these values, closed loop simulation of the proposed system is carried out. The GA simulation parameter values are listed in Table 2.

Parameter	Value
Population size	50
No. of generation	100
Range of K_p and K_i	0-5/0-10
Crossover ratio	0.8

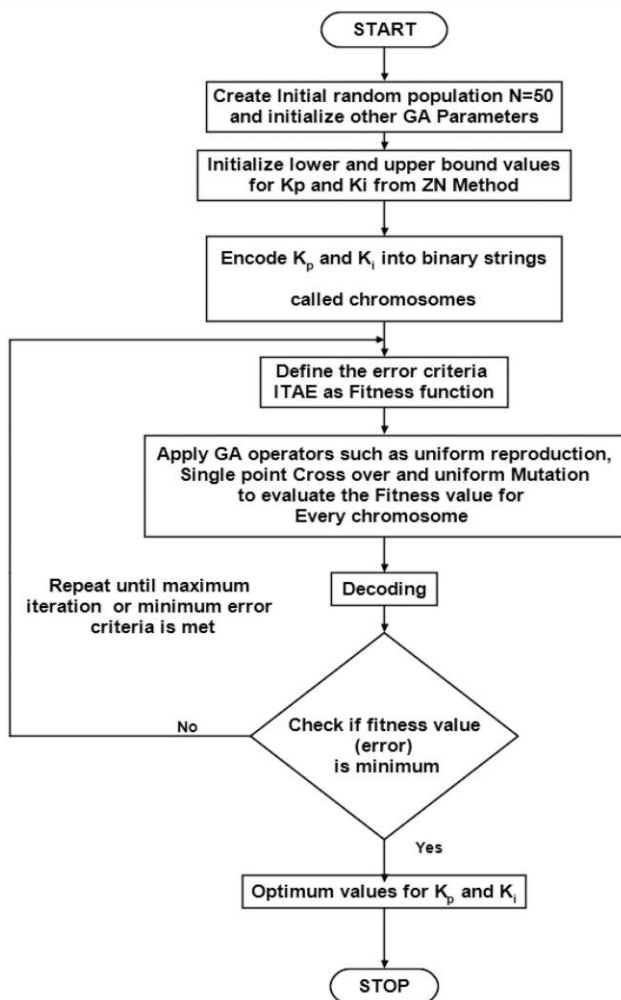


Fig-6 Steps of GA process

5. The analysis study of SEPIC using Matlab FFT analysis tool

Using the MATLAB simulation as shown in fig 4 we easily find out the THD of the SEPIC. Using PI controller harmonics is produced by SEPIC is near 1.5% which is limited under international electrical organisation standard. Hence we can say here that because of the low THD harmonics produce by SEPIC is negligible so supply in not pollute as compare to other and efficiency also not affected. Hence power factor of the supply is not disturbed and we get non inverted output with grate voltage stability. THD is show using FFT analysis of MATLAB in fig-7.

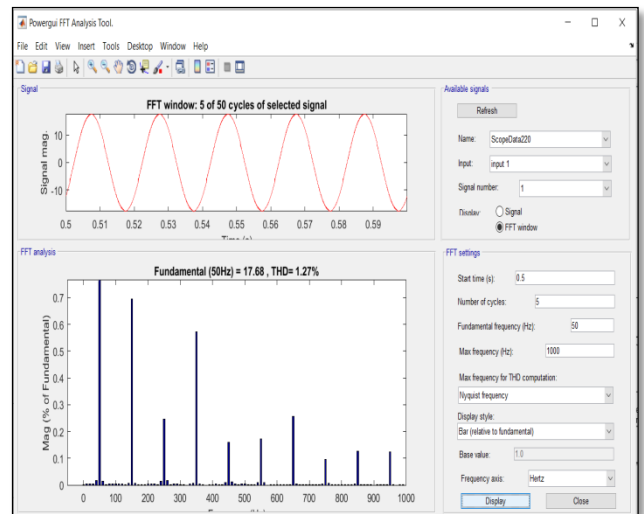


Fig-7 FFT analysis tools

6. Conclusions

In this proposed SEPIC dc to dc converter using PI controller which is the maintain the good power factor and eliminate the harmonics in the line current. This system simple but because of the SEPIC have fourth order system difficult to design controller for that. The closed-loop control of a SEPIC is designed using GA tuned PI controller system gives a robust performance with non-inverting output voltage.

In proposed system have two inductor and capacitor. Because of the capacitor C_1 SEPIC provided isolation to the input from output side because of that when we used for this in battery charging application it's not produce non-sinusoidal current which is affected power factor hence SEPIC is maintain and improve the power factor.

This dissertation work also have different basic converter which is helps us during the design of the SEPIC. Special cuk and SEPIC used for correction for PF but one difficult is felt in Cuk because cuk output is inverted while SEPIC gives non inverted output so it more robust and easy as compare to the cuk.

Hence for this all the advantageous point Single ended primary inductor dc to dc converter(SEPIC) is design for the correction of the power factor and more efficiency.

REFERENCES

1. N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications and Design. Hoboken, USA: Wiley, 2009.
2. Marian K. Kazimierczuk, "Pulse-width Modulated DC-DC Power Converter", John Willey & Sons, USA, 2008.
3. Limits for Harmonics Current Emissions (Equipment current $\leq 16A$ per Phase), International standards IEC 61000-3-2, 2000.

Type of controller	Rise time	Overshoot	Settling time	Steady state error
PI	Decrease	Increase	Small change	Eliminate

Table-3 PI controller analysis

4. Memon, A.H., Yao, K., Chen, Q., et al.: 'Variable-on-time control to achieve high input power factor for a CRM-integrated buck-flyback PFC converter', *IEEE Trans. Power Electron.*, 2017, 32, (7)
5. Dah, D., Ki, S.-K.: 'Light-load efficiency improvement in buck-derived single-stage single-switch PFC converters', *IEEE Trans. Power Electron.*, 2013, 28, (5), pp. 2105–2110
6. Poorali, B., Adib, E., Farzanehfard, H.: 'A single-stage single-switch softswitching power-factor-correction LED driver', *IEEE Trans. Power Electron.*, 2017, 32, (10), pp. 7932–794
7. da Fonseca, Z.P., Perin, A.J., Junior, E.A., et al.: 'Single-stage high power factor converters requiring low DC-link capacitance to drive power LEDs', *IEEE Trans. Ind. Electron.*, 2017, 64, (5), pp. 3557–3567
8. Liu, X., Xu, J., Chen, Z., et al.: 'Single-inductor dual-output buck-boost power factor correction converter', *IEEE Trans. Ind. Electron.*, 2015, 62, (2), pp. 943–952
9. Pereira, G.G., Dalla Costa, M.A., Alonso, J.M., et al.: 'LED driver based on input current shaper without electrolytic capacitor', *IEEE Trans. Ind. Electron.*, 2017, 64, (6), pp. 4520–4528
10. Umamaheswari, M.G., Uma, G., Annie Isabella, L.: 'Analysis and design of digital predictive controller for PFC Cuk converter', *J. Comput. Electron.*, 2014, 13, pp. 142–154
11. Ranganathan, G., Umanand, L.: 'Power factor improvement using DCM Cuk converter with coupled inductor', *IET Electronics Power Appl.*, 1999, 146, (2), pp. 231–236
12. Mahdavi, M., Farzanehfard, H.: 'Bridgeless SEPIC PFC rectifier with reduced components and conduction losses', *IEEE Trans. Ind. Electron.*, 2011, 58, (9), pp. 4153–4160
13. Poorali, B., Adib, E.: 'Analysis of the integrated SEPIC-flyback converter as a single-stage single-switch power-factor-correction LED driver', *IEEE Trans. Ind. Electron.*, 2016, 63, (6), pp. 3562–3569
14. Umamaheswari, M.G., Uma, G., Redlinevijitha, S.: 'Comparison of hysteresis control and reduced order linear quadratic regulator control for power factor correction using DC-DC Cuk converters', *J. Circuits Syst. Comput.*, 2012, 21, (1), p. 1250002
15. Kessal, A., Rahmani, L.: 'GA-optimized parameters of sliding-mode controller based on both output voltage and input current with an application in the PFC of AC/DC converters', *IEEE Trans. Power Electron.*, 2014, 29, (6), pp. 3159–3165
16. Sahid, M.R., Yatim, A.H.M., Taufik, T.: 'A new AC-DC converter using bridgeless SEPIC'. *IECON 2010 – 36th Annual Conf. on IEEE Industrial Electronics Society*, 2010, pp. 286–290
17. Gu, W., Zhang, D.: 'Designing a SEPIC converter', *Excellent Design Guidelines, National Semiconductor in Application Note*, April 2008, pp. 1–6
18. Designing DC/DC converters based on SEPIC topology By Jeff Falin Senior Applications Engineer Texas Instruments Incorporated *Analog Applications Journal*
19. T.M. Undeland, W.P. Robbins and N. Mohan, "Power electronics converters, applications and design," ed: New York [etc.]: John Wiley and Sons, 2003
20. S. Bacha, L. Munteanu, and A.L. Bratcu, *Power Electronics Converters modelling and Control*, Springer, 2014.