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DESIGN OF AN EFFICIENT VOLTAGE TO TIME CONVERTER FOR ECG ACQUISITION SYSTEM

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Abstract - *In VLSI, CMOS has become the prevailing technology because of its speed and the packing density which will be coupled with low power consumption. Conventionally, biomedical signal acquisition system generally consists of a low noise amplifier (LNA), an analog sample-and-hold, a band pass filter (BPF) and an Analog to digital converter (ADC). If these analog signals are converted to digital then they are susceptible to deleterious effects of additive noise. In conventional analog ECG acquisition system large capacitors are usually associated with it. It is clear that conventional ECG acquisition system is not desirable. So, the main goal is to reduce the power consumption and chip area. Here in this project, we will be designing a fully digital architecture by replacing the entire analog component with the efficient one that is fully in digital in order to achieve a better performance. This work will be done using Tanner EDA 16.3.*

Key Words: Voltage to time converter (VTC), Analog to digital converter (ADC), Bio signals.

1.INTRODUCTION

Biomedical signals are processed on a daily basis in hospitals. This is made possible because of the advances in integrated circuit fabrication. Health monitoring gadget is the result of this advancement in current trend. These gadgets are made as wearable so the wearer can feel comfortable with all this monitoring equipment. To implement this, bio signal processing is a must. Bio signals will be converted into digital. Conventional way of doing so is to use an ADC fig 1 to convert those analog bio signals into digital. It cannot be directly sent to ADC because the bio signal is usually corrupted because of the noise, and other hazard that are due to human activities. It should be amplified and filtered before converting. ADCs are usually associated with more power consumption because if the high supply voltage required. So, our main purpose of this work is to design a fully design ECG acquisition system that is compatible and efficient.

In various papers [1]-[5] different bio-signal acquisition systems were discussed. Fig. 1 is the conventional block diagram of ECG acquisition system. To remove the unwanted noise the amplified signal from the front-end architecture is given to the bandpass filter and then the analog signal is converted into digital by given the signal to ADC. This method is not desirable because of the large capacitors that are usually associated with AC coupling. Fig. 2 shows a chopper-based technique. This method is also not desirable because of the inability in low power design but the flicker noise is reduced. Fig. 3 shows a mixed signal feedback technique. This is a digital approach. Unwanted interfaces are removed when using this technique, but the amplifier that is used is analog. This block consumes lot of power thus limiting the performance benefits. Each mentioned design has an analog block and passive elements as a result the power and area associated with it is large. All these disadvantages can be eliminated by employing a fully digital approach. The signal processing will be done in time and digital domain. The analog signal will be converted into time domain with the help of VTC. The output of VTC is a time domain signal. This can be used to send to TDC to convert the time domain into digital domain.

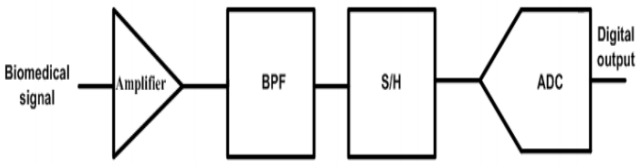

Fig 1: Conventional ECG Acquisiton System

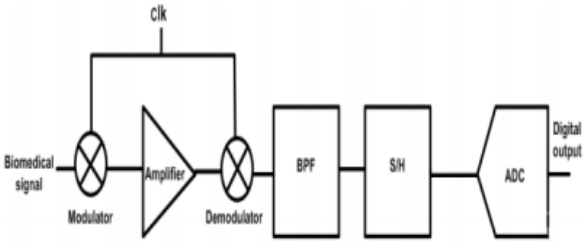

Fig 2: Chopper based ECG Acquisition System

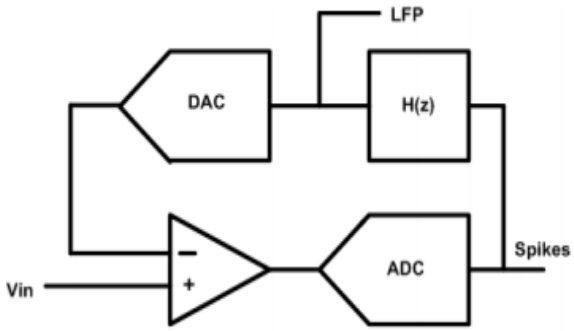

Fig 3: Mixed Signal feedback architecture

2. RELATED WORK

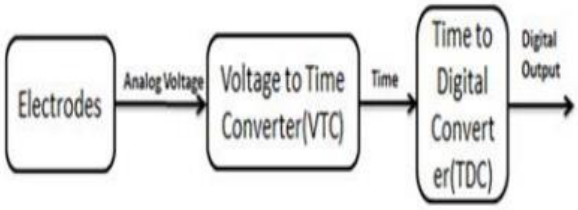

Fig 4: Digital Architecture

Fig. 4 is the block diagram of the digital system. It consists of Active electrode, Voltage to Time Converter (VTC) and Time to Digital Converter (TDC). As said earlier in Fig.4. Digital bio signal conditioning is done in the time and digital domain and supply voltage scaling will not affect the signal. Thus, CMOS technology seems to a good fit to design. Initially the ECG signal is given to the active electrode which almost act like a transducer and helps in converting ECG signal into electrical signal that are amplified. Active electrode [2] are made up of active elements that are intended to match with the high skin impedance. After this, the signal that is amplified is sent to the Voltage to time converter VTC to convert the signal into time domain. Then the signal is given to a Time to Digital Converter. In conventional design this conversion is usually down with the help of ADC but here in digital architecture this is done using VTC and TDC.

This would the flow diagram fig 5 for ECG acquisition system. The analog bio signal coming from that active electrode is directly connected to front-end circuit and is converted using voltage-to-time converter (Moving average) then that signal is passed to control logic which consists of a time comparator and SR latch. Then counter with D flipflop is placed after the control logic. The output of counter block is giver to either demur/decoder. And then finally a digital to current converter and again back to active electrode.

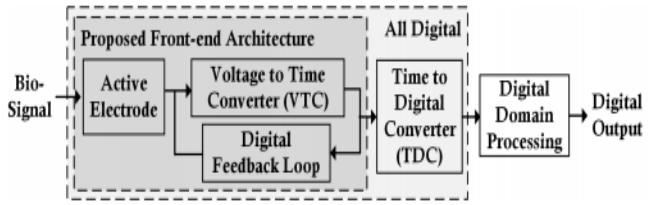

Fig 5: Design of fully Digital Architecture

3. VTC

In this, the processing of the bio-signal is performed in the time and digital domain, Hence the advantages of the digital CMOS technology are utilized. The analog bio-signal coming from the electrode is directly connected to the front-end circuit and is converted to time with a voltage-to-time converter (VTC). So, an efficient component of VTC is replaced with older one. Several VTC circuits have been introduced and the basic core used in the existing work was a simple current starved VTC but it faces some limitations like linearity, dynamic range and sensitivity.

To overcome that, first we have designed a differential current starved architecture which has many advantages. Here, the clock signal is used as pulse signal through an inverter consisting of MOSFETs.

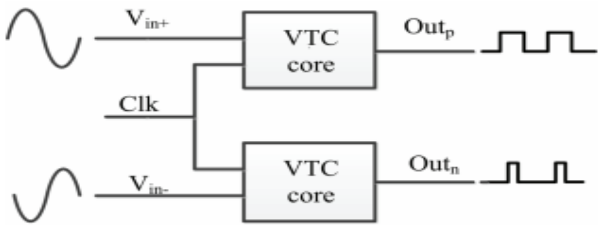

Fig 6: Differential current starved circuit

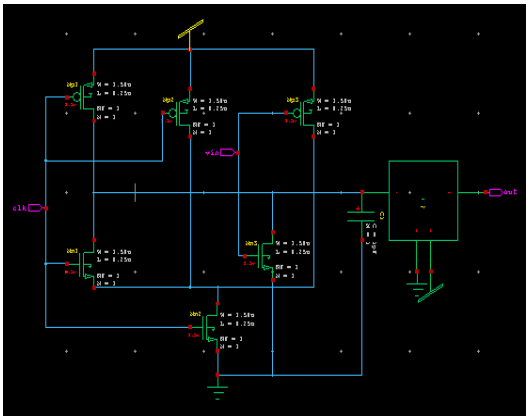

Fig 7: Core of the differential VTC

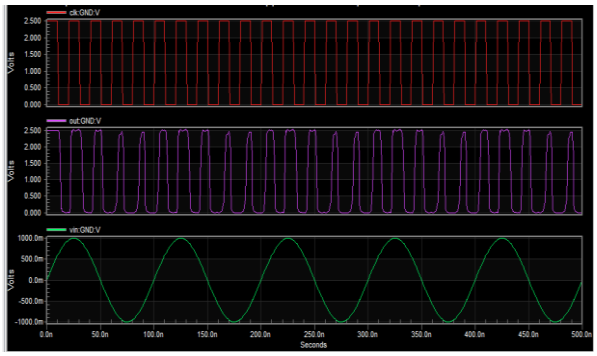

Fig 8: Simulation result for fig 5

Fig 7 shows the core of the differential VTC. This Core is derived from current starved inverter. Current starved inverter is a stacked structure. To eliminate the limitations of the input voltage, a folding structure is adopted. Using this new scheme dynamic range and linearity are further improved at high sampling rate.

Fig 8. The green colored wave is our input Vin with respect to ground and clock signal is displayed in red and finally this purple color is our output. The current starved inverter VTC, current starving means a technique to control an inverter delay by adding 2 more transistors.

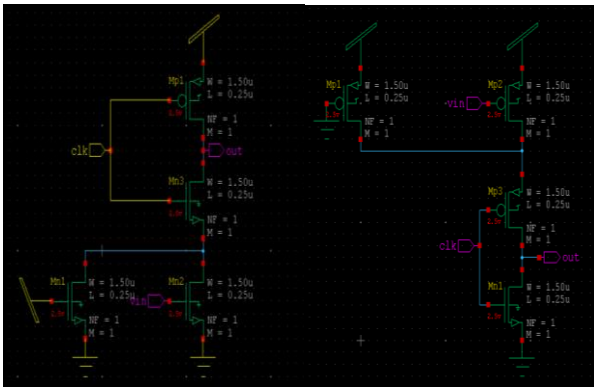

Fig 9: Current starved inverter VTC

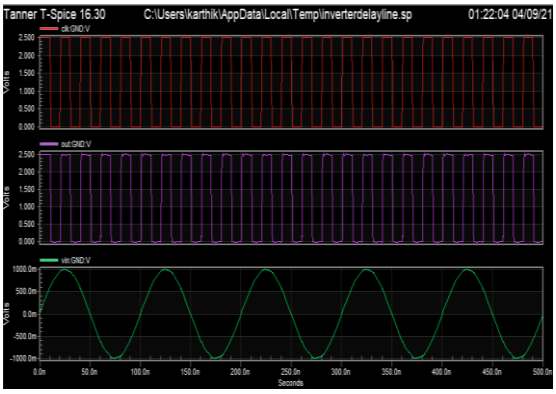

Fig 10. Simulation result for Current Starved inverter circuit

4.EXPERIMENTAL RESULTS

Now will see the circuit responses or the transient responses for the above circuits, where the power consumption and reduction in chip area would be our supreme aim of this project. So, according to the power analysis, in existing systems VTC (moving average) has got the highest power consumption compared to rest of the circuits.

TABLE-1: Power Report

Type Of VTC	Power consumed
Differential VTC	28.6mw
Current-Starved VTC	11.11mw
Moving-average VTC	55.66mw

Then the delay that too particularly single VTC block gives the total time taken in secs. Differential VTC has got less time compared to the rest of the circuit design.

TABLE-2: Total Time consumed Report

Type Of VTC	Total Time taken
Differential VTC	1.64 seconds
Current Starved VTC	1.84 seconds
Moving average VTC	23.44 seconds

Then, the count of MOSFETs that are needed to construct this design plays a crucial role. So, the differential VTC has got only 8 count.

TABLE-3: MOSEFT Count

Type Of VTC	Number of MOSEFTs
Differential VTC	8
Current Starved VTC	22

Moving average VTC	135

4. CONCLUSIONS

In the future expectation of the dominance of CMOS technology, in this work a digital architecture for ECG acquisition system is implemented. The simulation was carried out using Tanner tool with 250 nm technology. In conventional ECG acquisition systems, a normal ADC along with passive elements which requires high supply voltage was used which leads to high power consumption and area. In the proposed system, to reduce the power consumption and chip area we have designed a fully digital architecture by replacing a component with the efficient one in order to achieve a better performance. An active electrode which helps in offset cancellation is also introduced. Also, passive elements, LNA and analog filters are not used that leads to the reduction in chip area.

REFERENCES

[1] Maryam Zare and Mohammad Maymandi-Nejad," ECG Acquisition System with 0.5 V Supply," IEEE transactions on very large scale integration (VLSI) systems, Jan .2016

[2] J. L. Bohorquez, M. Yip, A. P. Chandrakasan, and J. L. Dawson, "A biomedical sensor interface with a sinc filter and interference cancellation," IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 746–756, Apr. 2011..

[3] R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm2,5μW, DC-coupled neural signal acquisition IC with 0.5 V supply," IEEE J. Solid-State Circuits, vol. 47, no. 1, pp. 232–243, Jan. 2012.

[4] Channappa Bhyri, Kalpana, V, S. T. Hamde and L. M. Waghmare, Estimation of ECG features using LabVIEW, International Journal of Computing Science and Communication Technologies, Vol. 2. No. 1, 2009, pp. 320-324.

[5] Alice de Jesus Kozakevicius, Cesar Ramos Rodrigues, Raul Ceretta Nunes, Roberto Guerra Fillo, Adaptive ECG filtering and QRS detection using orthogonal Wavelet transform, in Proceedings of the Biomedical Engineering (BioMED' 2005), 16 – 18 February, 2005, Innsbruck, Austria.

[6] J. S. Sahambi, S. N. Tandon and R. K. P. Bhatt, A new approach for on-line ECG characteristics, pp. 409- 411.

[7] Juan Pablo Martinez, Rute Almeida, Salvador Olmos, A Wavelet Based ECG Delinator: Evaluation on standard data bases, IEEE Transactions on Biomedical Engineering, Vol. 51, No 4, 2004, pp. 570-581

[8] . S. Z. Mahamoodabadi, A. Ahmadian, M. D. Abolhasani and M Eslami, ECG Feature extraction based on multiresolution wavelet transform, in Proceedings of the 27th IEEE Annual Conference of the' Engineering in Medicine and Biology', 2005, pp. 3902-3905

[9] H. Gholam Hosseini and H. Nazeran, Detection and extraction of the ECG signal parameters, in Proceedings of the 20th IEEE Annual International Conference on Engineering in Medicine and Biology', 1998, Vol. 20, No. 1, pp. 127-130

[10] Mihaela Lascu and Dan Lascu, LabVIEW Electrocardiogram Event and Beat Dection, WSEAS Transactions on Computer Research, 2008, Issue 1, Vol. 3, pp. 9-18.

[11] S. S. Mehta, S. C. Saxena and H. K. Verma, Computer aided interpretation of ECG for diagnostics, International Journal of System Science, 1996

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