International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 08 Issue: 05 | May 2021 www.irjet.net p-ISSN: 2395-0072

DESIGN OF COTS BASED DRAM MEMORY MODULE FOR SPACE APPLICATION

Dr. N. Nagaraju[1], S. Shobana[2], G. Siva Ranjani[3], S. Sivagami[4]

[1]Associate Professor, [2, 3, 4]UG Scholar, Department of Electronics and Communication Engineering Adhiyamaan College of Sump, Tamilnadu, India.

[1]nnagaece@gmail.com, [2]shobanasambath15@gmail.com, [3]sivaranjanig2000@gmail.com, [4]shansivagami29@gmail.com

---

Abstract - *The on-board computing capabilities of spacecraft are a significant limiting issue for accomplishing several categories of future missions. Above all, the foremost space exploration program needs effective execution of data-intensive operations, like navigations, terrain relative navigation, hazard detection and avoidance and scheduling. In the existing system, we designed a radiation tolerant stacked memory array based on state-of-the-art chip stacking. Our module can be directly connected to a host processor and act as a highly reliable DDR3 module. In the proposed system, rewiring-based memory stacking is developed using the symmetric stacking of flip flops and logical elements. The proposed casting of DRAM evaluates the deep-driven architecture with reduced logical space. The built-in self-test showing the logical compression is simulated and displayed.*

Key Words: DDR, Build in self-test, DRAM, COTS.

1. INTRODUCTION

Rapid advances in the areas of deep-submicron electron technology and design automation tools are enabling engineers to design larger and more complex circuits and to integrate them into a single chip. System on chip (SOC) design methodology is seen as a serious new technology and therefore the future direction for semiconductor industry. The most important challenges for SOC testing are linked for test cost and fault coverage. According to the ITRS (International Technology for Roadmap Semiconductors) by 2014 it may cost more to test a transistor than to manufacture it unless techniques like logic Built-In-Self-Test (BIST) are employed. BIST may be a technology to maneuver on board the most functionalities previously administered by Automated Test Equipment (ATE). In traditional BIST architectures, test pattern generation is usually performed by adhoc circuitry, typically Linear Feedback Shift Registers (LFSR), cellular automata and multifunctional registers like BILBO (Built-In Logic Block Observer). BIST involves using on-chip hardware to apply pseudorandom test patterns to the Circuit Under Test (CUT) and to analyze its output response. The most widespread approach is test-per-scan BIST scheme. Unfortunately, many circuits contain random-pattern-resistant faults which limit the fault coverage that will be achieved with this approach. One method for improving the fault coverage for test-per-scan BIST is to modify the CUT by either inserting test points or by redesigning it to improve fault coverage. The drawbacks of those techniques are that they typically add additional logic levels to the circuitry which will degrade system performance. Fault coverage are improved differently by using weighted pseudorandom sequences. Additional logic is required to weight the probability of every bit within the test sequence. The weight logic is often placed either at the input of the scan chain or within the individual scan cells. The disadvantage of probability weighting approach is within the need of storing of the load sets on chip and also, control logic is required to modify between weights, so the hardware overhead may be large. A third method to enhance the fault coverage is to use "mixed mode" approach where deterministic patterns won't detect the faults that the pseudorandom patterns miss. Storing deterministic patterns may require outsized amount of hardware overhead. In a technique based on reseeding an LFSR was proposed that reduces the storage requirements. Therefore, another improved technique was developed that uses the multi polynomial LFSR for encoding a group of deterministic test cubes.

2. METHODOLOGIES

2.1 COTS Solution

The mentioned issues rationalize a 3-D-M3 of COTS memory with a custom RHBD controller. COTS devices have tons of scrutiny and interest within the space community. Extensive testing on SDRAM COTS has been undertaken over the recent years and NASA successfully used them in spacecraft for critical applications like for the Compute Element within the Mars lab Curiosity rover. With proper component screening and radiation testing, the utilization of COTS devices within our cube provides a low-cost and

effective the solution to capture the advantages offered by state-of-the-art commercial devices.

2.2 OUR 3-D MEMORY CUBE SOLUTION

Selecting the foremost radiation-tolerant, high-performance COTS memory available, stacked using the proposed technology and integrated with the controller chip, will render the 3-D architecture resilient for the space environment while retaining state-of-the-art performance in terms of bandwidth and density. More than theoretically achieving comparable performances to the HMC, our solution also offers increased density, possible intermixing of different memory types such as magneto resistive random-access memory (MRAM), NAND Flash, etc. into one cube, increased fault-tolerance aspects like individual die access, also as avoidance of TSVs use for interconnection between dies.

3. PREVAILING SYSTEM

A device core testing logic or we call it a built-in-self test of analog signals with minimal area overhead for measuring on chip voltages in all-digital manner is meant here. The tactic is fitted to a distributed architecture, where the routing of analog signals over long paths is minimized. A clock is routed serially to the sampling heads placed at the nodes of analog test voltages. This sampling head present at each test node, which consists of a pair of delay cells and a pair of flipflops, locally converts the test voltage to skew between a pair of subsampled signals, thus giving rise to as many subsampled signal pairs. To live a particular analog voltage, the corresponding subsampled signal pair is fed to a delay measurement unit to live the skew between this pair. The concept is validated by designing a test contribute UMC 130-nm CMOS process. Sub-millivolt accuracy for static signals is demonstrated for a measurement time of a couple of seconds and an efficient number of bits is demonstrated for low bandwidth signals within the absence of sample-and-hold circuitry.

In the proposed system, a Built-In-Self test is performed by employing a sample module also known as random access memory. The BIST RAM is taken into account under test and different advance test cases are given to check the circuit. The performance is measure in such how the facility consumption reduction and area efficiency is achieved. Bias variations are a standard problem in analog circuits and are becoming worse because of the technology scales. This is because, the method variation is increasing and therefore the power supply is reducing. With the increasing popularity of mixed-signal IC designs within the deep-submicron processes, it is of interest to exactly measure the analog voltages for test and debugging purposes. Such situations arise when measuring on-chip voltages for built-in-self test (BIST). The analog voltages might be potentially located everywhere on the chip. It's desirable that the measurement circuitry employed in such situations occupies as small a neighborhood as possible and is straightforward to style. In the proposed architecture, the dc voltages of the test nodes are all tied together to a standard bus and digitalized centrally to a digitizer (ADC). Even ac signals are converted to dc through an envelope detector, but calibration is required during this case to map the digitized values to analog amplitude. In such cases, one has got to know the amount of sensor nodes beforehand or design for a worst-case scenario to make that the worth on the bus settles within a specified time. Also, for the ac case, calibration puts a boundary on the testing time required.

In the proposed system, rewiring based memory stacking is developed using the symmetric stacking of flip flops and logical elements. The proposed casting of DRAM evaluates the deep driven architecture with reduced logical space and area utilized. The built-in self-test showing the logical compression is simulated and displayed.

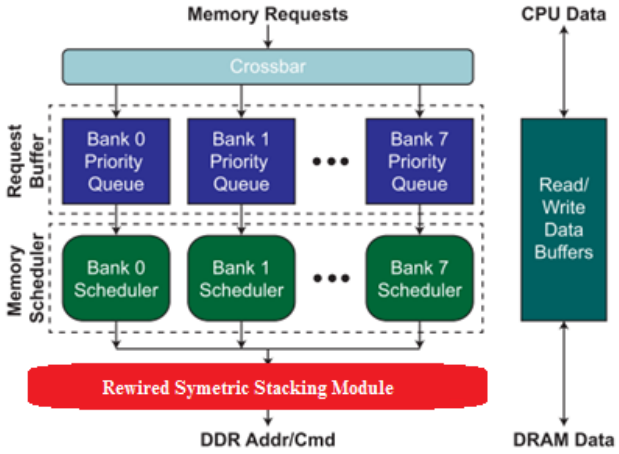

Fig 1: DRAM memory module

In the proposed system, rewiring based memory stacking is developed using the symmetric stacking of flip flops and logical elements. The proposed casting of DRAM evaluates the deep driven architecture with reduced logical space and area utilized. The built-in self-test showing the logical compression is simulated and displayed.

4. TESTING ALGORIYHMS

4.1 Checker Board Test

It is exactly sort of a chessboard which has alternate blocks of black and white, likewise, alternate values sequence like the "10101010101010101010" pattern is being loaded at high frequency and skim in high frequency. Just in case of any silicon, level fault exists in memory the results of this test turn positive indicating Fail

4.2 Marching Test

It is nothing but the action of March fast. The info is being loaded into the memory forward direction like March fast, in regular intervals with reference to clock. The info is read from the memory and given for validation. Just in case of any silicon, a level fault exists in memory the results of this test turn positive indicating Fail

4.3 Pattern Test

It is purely an optional test that's want to test the memory for silicon level issues by writing a hard and fast pattern of knowledge like “11001100” or “11111110” or “10100000” etc. this type is of operation helpful for the memory to check if any logical mistakes exist in memory. Just in case of any silicon, a level fault exists in memory the results of this test turn positive indicating Fail

4.4 Pseudorandom Test

Pseudo – Repeated Random – Undetermined

Repeated random numbers are more accurate and specific when considering the testing of a tool. This type of knowledge is generated during a fixed interval at high frequency and loaded into the memory. Just in case of any silicon, a level fault exists in memory the results of this test turn positive indicating Fail

5. RESULT AND DISCUSION

The designed system is under a build-in test case, that provides a design flow and used through Xilinx ISE software to analyze the characteristics. The green color waveform produced is the simulated flow of the memory module. The 8-bit input is given and the output is produced and indicated in simulation result.

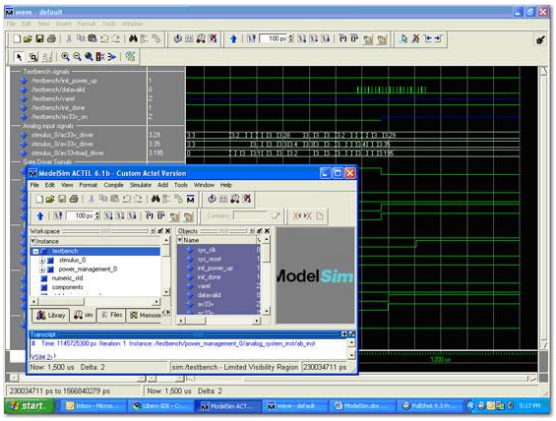

Fig 2. Xilinx and Modalism

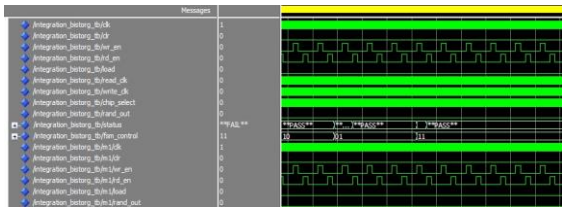

Fig 3. Status of memory

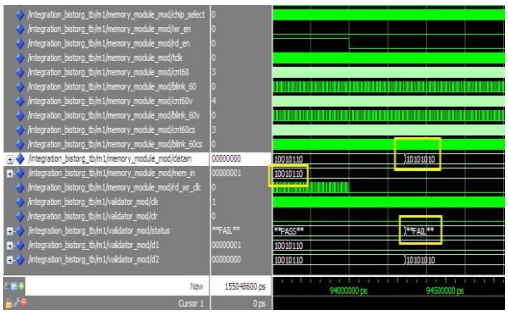

Fig 4. Waveforms for data_in and memory_in

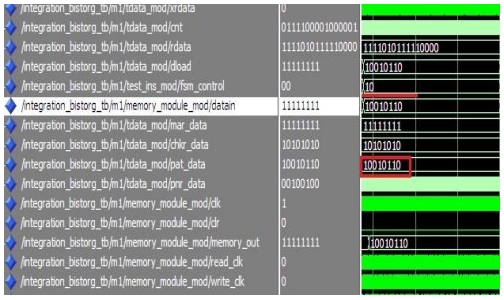

Fig 5. Simulation results with testbench

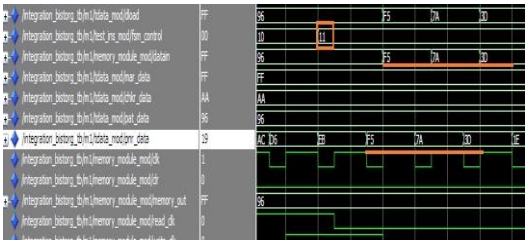

Fig 6. Simulation results with read and write counts

5.1 Tabulation

The efficiency of designed system over the existing system is tabulated. The parameters like Read and Write counts, the total number of instructions, simulation time, MIPS and MTPS are compared. The read and write and the number of instructions is same but the simulation time is reduced than the previous model. Similarly, the MIPS and MTPS shows efficiency in overall operations.

	EXISTING SYSTEM	PROPOSED SYSTEM
Sequential Read after Write	2000	2000
Total number of instructions	3300	3300
MIPS	16,35	19,13
Simulation time(ns)	201850	172525
Mega transactions per second	9,91	11,6
Consumed bandwidth (Mpbs)	317,07	370,96

Table -1: various parameters are compared over the existing system.

6. CONCLUSIONS

The prevailing system designed by using a stack of flipflop. This arrangement allows us to processing the data as fast than the other existing models. The simulation time where reduced and the other parameters are discussed. The overall output shows the efficiency of this model. The design done by the Xilinx software which gives the waveform and the modalism shows the dataflow of the 3D-DRAM module.

REFERENCES

[1] A. Agnesina et al., "A novel 3D DRAM memory cube architecture for space applications," in Proc. 55th ACM/ESDA/IEEE Design Autom. Conf. (DAC), Jun. 2018, pp. 1–6.

[2] D. U. Lee et al., "25.2 a 1.2 V 8Gb 8-channel 128GB/s high-bandwidth memory (HBM) stacked DRAM with effective microbump I/O test methods using 29 nm process and TSV," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2014, pp. 432–433.

[3] J. T. Pawlowski, "Hybrid memory cube (HMC)," in Proc. IEEE Hot Chips 23 Symp. (HCS), Aug. 2011, pp. 1–24.

[4] S.-K. Lim, "Bringing 3D ICs to aerospace: Needs for design tools and methodologies," J. Inf. Commun. Converg. Eng., vol. 1, no. 2, pp. 117–122, Jun. 2017.

[5] P. M. Gouker et al., "SET characterization in logic circuits fabricated in a 3DIC technology," IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2555–2562, Dec. 2011.

[6] R. K. Kirschman, "Low-temperature electronics," IEEE Circuits Devices Mag., vol. 6, no. 2, pp. 12–24, Mar. 1990.

[7] [7] R. K. Kirschman, "Low-temperature electronics," IEEE Circuits Devices Mag., vol. 6, no. 2, pp. 12–24, Mar. 1990.

[8] [8] TN-41-01: Calculating Memory System Power for DDR3, Micron, Boise, ID, USA, 2007.

[9] [9] Y. Lin and J. C. Joy, "A new examination of secondary electron yield data: Surface and interface analysis," Int. J. Devoted Develop. Appl. Techn. Anal. Surf, Interfaces Thin Films, vol. 37, no. 11, pp. 895–900, 2005.

[10] [10] M. Park et al., "Soft error study on DDR4 SDRAMs using a 480 MeV proton beam," in Proc. IEEE Int. Rel. Phys. Symp. (IRPS), Apr. 2017, p. SE-3.

BIOGRAPHY:

Dr. N. Nagaraju,
Associate Professor,
Electronics And Communication Engineering Department,
Adhiyamaan College of Engineering,
Anna University.