Physical Design of 32-bit RISC-V Processor

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Abstract - *A method to implement the physical design of 32-bit RISC-V processor is proposed. Physical design implies the design collecting and availability of computerized netlist of an IC say a processor, by meeting the plan determinations like planning, force and territory. physical design is done using cadence tool using ASIC flow.*

***Key Words*: (RISC-V (Reduced Instruction Set), Bit manipulation instructions, ALU (Arithmetic and Logical Unit), Verilog, Cadence, Genus.**

1.INTRODUCTION

The RISC-V ISA is free, open, and particular. It claims to keep away from steady turn of events and changes rather than restrictive ISAs. It works on little code sizes, detach design from execution, and leave space for development. The RISC-V ISA has just observed a few usages just as real silicon (for example ASIC – Application specific integrated Circuit). The netlist generated after the synthesis of Verilog HDL code in the cadence tool with 45nm technology is used for physical design. The modules instantiated in top level module.

2. LITERATURE SURVEY

Risc-v offers simple, modular ISA
RISC-V is simpler to execute than certain other options, negligible RISC-V centers are generally 50% of the size of comparable ARM centers and the Instruction Set Architecture has just accumulated some help from the semiconductor business.

RISC-V is a universally useful instruction set architecture that is BSD authorized, extensible and eminence free.

1. RISC-V's particular ISA offers numerous choices.
2. The RISC-V location space is byte numerous choices.
3. The base instruction set is straightforward and smoothed out, permitting effective negligible execution.
4. RISC-V incorporates three floating point extensions. They are as per the following;
    - Single precision
    - Double precision
    - Quadruple precision

Based on early turns of events, RISC-V instruction set architecture shows up promising. It offers all the essential RISC highlights and a couple of turns that streamline the usage, there by lessening die zone and conceivably power utilization.

Analysis on the possibilities of RISC-V adaption

- As the interface among hardware and software, instruction set architecture assume a vital job in the activity of computers. While both hardware and have kept on advancing quickly over the long run, instruction set architectures have gone through negligible change.
- Set up on the chief of the Reduced Instruction Set Architecture (RISC), and as an open-source ISA, RISC-V offers numerous advantages over mainstream ISA like Intel's x86 and ARM holding's advanced RISC machine.
- Instruction Set Architectures (ISA) are executed straightforwardly onto the processor during assembling. Accordingly, the decision of ISA characterizes the kinds of essential guidelines that the processor can decipher.
- As Moore's law eases back and processor productivity searches for alternate approaches to improve, the business may turn to RISC-V usage to improve equal handling execution.
- The business may go towards actualizing software RISC-V design because of its open-source nature.

Towards high performance RISC-V emulator
Having a high-performance RISC-V emulator for regular designs, for example x86, ARM, would encourage its appropriation and testing as well as would show it as a helpful virtual design to ease programming arrangements. One way to deal with implement an elite emulator is by utilizing Dynamic Binary Translation.

1. RISC-V configuration used in this experiment and the SBT (Static Binary Translation) usage, they have used the RISC-V 32-bit instruction set, fundamentally to
    - Encourage examinations with open ISA, that is likewise 32-bit.
    - Encourage interpretation to ARM 32 cycle.
2. The standard RISC-V instructions utilizes by them are multiplication and division instructions, single and double precision floating point.
3. To evaluate the performance overhead introduced by the SBT (Static Binary Translation), we think about the execution of benchmarks copied with SBT against the performance of their local execution.

Extensions for Bit Manipulation Instructions

The areas like machine learning and cryptography includes operations on bits of a register. Therefore, bit manipulation instructions (BMI) become crucial in embedded systems and 10 BMI is included to the existing RISC-V ISA (Instruction Set Architecture) BMI (shift left and shift right). To be more precise the instructions are compared with X86 and ARM instructions which are used by most of the processors.

The instructions included are as follows:

1. Parity: It checks if the number of bits is even or odd in a register.

2. BSWAP: This instruction concerts the data from little-endian to big-endian or vice versa

3. Rotate left: Shifting of data in cyclic order through left

4. Rotate right: Shifting of data in cyclic order through right

5. Pop count (POPCNT): Used to count the number of 1 bit in a register

6. Parity: It checks if the number of bits is even or odd in a register.

7. BSWAP: This instruction concerts the data from little-endian to big-endian or vice versa

8. Rotate left: Shifting of data in cyclic order through left

9. Rotate right: Shifting of data in cyclic order through right

10. Pop count (POPCNT): Used to count the number of 1 bit in a register

11. CLZ (count lead zero): This will count the number of leading zero bits

12. CTZ (count trailing zero): Counting the number of trailing zeros

13. PEXT (parallel extract): For extracting the one-bit field

14. PDEP (parallel deposit): For one bit field

15. BREV (bit reverse): To reverse the several bits in a data

Open-source RISC-V Processor IP Cores for FPGA- Overview and Evaluation. Use of FPGA is increasing, so it is a useful task to select a core intellectual property (IP) in order to reach the design specifications. So, an overview and evaluation for the selection of an CPU/IP core is given.

IP cores, ISA also come into picture along with it as it provides a bridge between hardware and software in the processor.
So, they have selected RISC-V ISA as it is an open source. They have taken few open cores available and after evaluating them they have given some of the points that has to be considered while selecting an open core

They are as follows*:*

1. The ISA and the IP core should be open source.
2. There should be a System-On Chip(SOC) bus interface
3. The IP core should use a single edged clock and a wide reset signal.
4. Source code should be technology and tool independent
5. ISA should be supported by a standard C/C++

A 45nm 1.3GHz 16.7 Double-Precision GPLOPS/W RISC-V Processor with Vector Accelerators

The speed is an important criterion with respect to the processors. Researchers have implemented a dual-core processor using the accelerators like rocket scalar core and Hwacha vector accelerators.The chip is implemented using ASIC flow. The rtl is written in HDL (Hardware Description language) and it is verified using C++ cycle simulator. The tool used for physical designing is ASIC CAD tool.

It is mapped to the Verilog generated by the HDL. After the implementation the power, area, frequency and the energy efficiency are calculated.

Design of pipelined RISC MIPS processor using VLSI

The principal point is to plan and actualize RISC MIPS processor utilizing VLSI innovation. The venture includes recreation and combination. The processor is planned with Verilog HDL, integrated utilizing XILINX.

RISC for load and store separate instructions utilized, and to speed up access of memory more than once, separate register bank is planned. The target of task is to speed up and lessen the power utilization.
Five pipelined stages are used they are:

a) Instruction fetch
b) Instruction decode
c) Execute stage
d) Memory access
e) Write backstage

RISC-V microarchitecture processor and its FPGA type

Opensource RISC-V (RV32I) ISA and development of synthesizable 32-bit processor is introduced. RISC-V instruction set design (ISA) is currently liberated to turn into an open design for scholarly and mechanical applications, For the achievement and selection of RISC-V, it has been intended to support for 32-bit, 64-digit and 128-cycle address spaces. Hardware design architecture to figure it out RV32I base integer instruction set for 32-bit address space is presented. single core, non-bused based, single cycle architecture with full help for RV32I base integer instruction set is implemented

Simulation environment:

Assembly code of instruction into binary is converted by assembler, this data is stacked to the instruction memory for the execution. At that point the given program is tried utilizing the simulation environment. After approval the processor was prototyped on FPGA with the outcomes showed on the LCD. The depiction of core was fabricated utilizing Verilog HDL. Xilinx ISE 14.7 was utilized for blend furthermore, FPGA prototyping. Maximum operating frequency is 32MHz. The power consumption is 7.9mW using Xilinx Power Analyzer. The benefit of the developing RISC-V people groups along with the current device chain and programming around this new instruction set and dependent on this plan worldview, the current processor configuration makes ready of future usage for explicit and general applications in the IoT and real-life embedded applications.

Design and evaluation of small float SIMD extensions

The set of extensions for RISC-ISA to support smaller than 32 bits FP formats on embedded processors is proposed. Scalar operations are supported by set of ISA extensions corresponding to new formats namely " xf16"," xf16alt"," xf18".and these extensions can be remembered for any RISC-V usage without loss of consistence with standard. Scalar extensions are provided that match the operation available in “F” and “D” standard extensions. Furthermore, optional vectorial extensions are specific which make use of SIMD sub-word parallelism on the FP register file. Lastly there is an optional extension for auxillary operations.The smallFloat extensions can be included in any RISC-V implementation without loss of compliance with the standard.
Low power implementation of RISC-V processor

- The board of intensity is compulsory for all plans of 90nm and beneath in light of the fact that with the shrinkage of gadget calculations the spillage current increments quickly.
- The administration of this spillage current has high impact on the plan just as the execution decisions, with respect to not many libraries and plans, spillage currently well performed .
- As of recently the essential concern was to improve execution in the plans and decreasing silicon necessity hence bringing down assembling costs yet this pattern is losing to control the board as the critical worry in SoC(System On Chip) planning.

The primary thought is to have the proficient low force RISC-V processor with DFT. The following force the board strategies for exchanging and spillage power decrease are being applied to the plan

I. Multi-V_{th}

ii. Clock Gating and Clock Tree Optimization

iii. Multi-supply voltage

iv. Power Shut Off (PSO)

Physical design implementation of single core 32 bit RISC processor on 28nm technology

Usage of 32Bit RISC Processor here began with Design netlist which contains data of the cells utilized, their interconnections, territory, and different subtleties, this plan netlist is blended methods imperatives were applied to guarantee the plan meets the usefulness and speed.

Subsequent stage was floor arranging in this pass on and center territory are made as for perspective proportion and usage factor and afterward dependent on the macros present that put the macros in brilliant manner so that in additional stages there are no clogs.

At that point parceling was done to separate the chip into little squares after that force arranging was done further prior to doing arrangement, all Wire Load Models (WLM) were eliminated as situation utilized RC esteems from Virtual Course (VR) to ascertain timing.

Position was done as pre-arrangement, in situation and post many arrangements advancement Clock tree union was done to adjust the slant and limit the inclusion delay after CTS Routing was done which is partitioned into two worldwide and point by point directing as this is done further need to do look and fix and cells later need to do ECO checks, for example, timing ECO, useful ECO, metal ECO, power ECO and Clock ECO. As this actual plan steps are done need to do actual confirmation as it checks the rightness of the produced format plan.Finally see Graphic Database System (GDS II) document, it is information base record design which is industry standard for information substitute of IC format craftsmanship.

Physical Design Implementation of 32 bit RISC processor Subsystem

- Reduced Instruction Set Computer (RISC) is a processor with less guidelines and less intricacy.
- The underlying advance of Physical Design is imp
- The RISC processor's Physical Design usage is finished by playing out every single check during floorplan, position, CTS and routing. At every single stage infringement are fixed by applying the comparing techniques. In arrangement stage GRC blunders are diminished to permissible range. In CTS slant is minimized. Shorts are fixed in directing stage.
- Timing infringement are fixed in the ECO stage.
- orting all the sources of info records like Netlist, Standard Design Constraints (SDC), Libraries (Logical and Physical) plan cycle begins by considering this data follows further PD stages beginning with Floor plan.
- GRC infringement are decreased from 87 to 28. In directing DRC are decreased from 17 to 10 and also all are diminished by repairing short. set

infringement revealed are 64 and are reduced similarly 88 hold infringement are fixed in the last stage.

3. CONCLUSION

A RISC-V Processor is open source which adds an advantage for using it. The source code can be modified depending on the applications. A 32-bit RISC-V Processor has been implemented with some extended blocks to the source code. The RISC architecture is simulated in Cadence RTL Compiler and synthesized using Genus tool.

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