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Design and Implementation of Trinary Cascaded 9- Level H-Bridge Inverter

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Abstract - *A multilevel inverter having more number of levels is responsible for reducing the harmonic content in output voltage as harmonics which are present in AC supply which leads to heating of equipment & sometimes causes mal operation of equipment. Trinary cascaded H bridge 9-level inverters operated using unequal input DC power sources with less number of switches. The operation principles and current conduction paths are analyzed in detail and phase disposition sinusoidal pulse-width modulation is used for voltages. As compared to other nine level inverters suitable for low-voltage applications , this inverter has advantages in a number of gate drivers, a number of dc sources, and efficiency. Simulation and experimental results under different settings of modulation index, switching angles and load are presented to verify the effectiveness and performances of the proposed inverter.*

Key Words: Multilevel, Cascaded, Trinary, Harmonics Genetic Algorithm.

1. INTRODUCTION

Harmonics are unwanted higher frequencies. When these unwanted higher frequencies superimposed on the fundamental waveform , it creates distorted wave pattern. These harmonics are generated because of electronic equipment with nonlinear loads. The short pulses causes distorted current waveform which in turn cause harmonic currents to flow back into other parts of the power system. These current harmonics distort the voltage waveform and causes distortion in the power system which can cause many problems. The performance of power system is badly affected by the generation of harmonics in power system. So to increase performance and efficiency of power system we need to minimize THD (Total Harmonic Distortion) losses and improve overall power quality of AC supply.

The proposed technique is brought into use to eliminate the traditional logic gate pulse technique which is conventional method. There is a pulse generator for giving pulses to the switches which is designed by Genetic Algorithm. A multilevel inverter having more number of levels can be responsible for reducing the harmonic content in the voltage at output. A multilevel inverter is a power electronic device which is based on semiconductor. It is used for high-power, high-voltage applications. Conventional two level inverter have some boundaries in high-power and maximum - voltage applications through switching losses and power ratings. The multi-level inverter has been introduced since 1975 as an alternative in high power and medium voltage conditions. The Multilevel inverter is like an inverter and it is used for industrial applications as an alternative in high power and medium voltage situations .To achieve smooth and least distorted dc to ac conversion and it can produce a multiple step voltage waveform with minimum distortion ,less switching frequency and efficiency.

Cascaded Trinary H-bridge multilevel inverters are designed using unequal input DC power sources with less switches.To obtain a large number of output voltage levels with least devices, it presents a cascaded H-bridge multilevel inverter using trinary dc sources. The future inverter can create high quality output voltage near to sinusoidal waves. The circuit configuration is simple and easy to control. The operational principle and key waveforms are illustrated and examined. If DC voltage sources having the ratio of 1:3, then the inverter is called as trinary asymmetric multilevel inverter. Genetic Algorithm is used to implement this topology. Binary asymmetric multilevel inverter produces seven level output which requires 8 switching devices. Trinary asymmetric multilevel inverter can produce nine levels but having same switching devices. Other techniques as fuzzy logic also can be used with such converters. Based on the modulation index as input, rules of the fuzzy logic controller (FLC) opens various possibilities in producing pulses directly But this paper explains the GA technique for inverter operation. Using the same number of switches is the advantage of a trinary asymmetric topology over a binary asymmetric topology. However such kind of multilevel inverter will require input DC voltage sources having different values.

1.1 DESIGN STEPS

Design of single phase trinary 9-level inverter is totally depends upon the voltage levels. The value for each DC source can be obtained from the Equation,

$V_K = 3^{(k-1)} V_{dc}$, k = 1,2,3,.....h (1)

Number of voltage levels N_L are obtained as,

$N_L = 3^h$ (2)

'N_S' is Number of switching devices,

$N_S = 4h$ (3)

'V_O max' is Maximum output voltage,

$V_O \max = (3^h - 1) V_{dc}/2$ (4)

Hence for 9 level inverter there is need of two different input dc source and 8 switches. Circuit diagram of the inverter is shown in fig 1. It is having two bridges, bridge one having the input voltage as V_{dc} /4 and the second one is having 3 V_{dc} /4 The voltage levels are shown in figure 2.

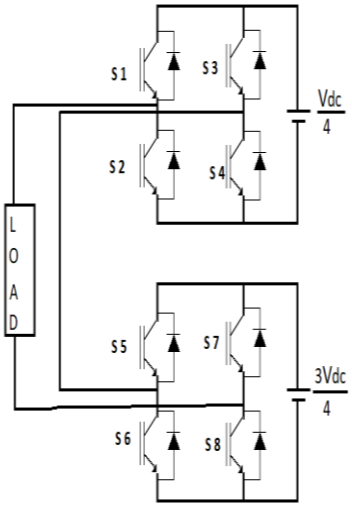

Fig. 1 : Trinary 9-Level Inverter

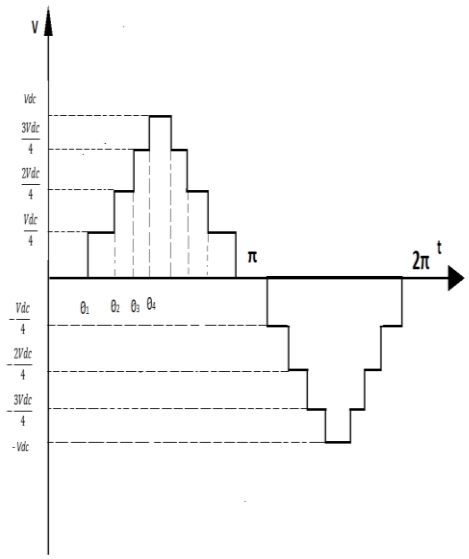

Fig. 2 : Voltage levels with respect to firing angles

By opening and closing of the switches of bridge-1 properly, an output voltage V1 is can be made equal to V_{dc} /4, 0, V_{dc} /4 and while an output voltage of bridge-2 is can be made $3V_{dc}$/4, 0 or $3V_{dc}$ /4 by closing and opening its switches. Therefore at the output, the voltage of the inverter ishaving the nine values V_{dc} /4, $2V_{dc}$ /4, $3V_{dc}$ /4, V_{dc}, 0, V_{dc} /4, $2V_{dc}$ /4, 3 V_{dc} /4, and V_{dc}. By using genetic algorithm the firing angles for the switches can be calculated. For better performance modulation index is selected 0.9. The required firing angles are calculated and they are shown in the following table. Where $\theta 1 < \theta 2 < \theta 3 < \theta 4 < \pi/2$.

The maximum fundamental voltage (V1max= 4Vdc/4) can be obtained when all of the switching angles are zero. The equation for ma is given below.

$$m_a = \frac{\pi V1}{4sVdc} \quad (5)$$

from this the following equations can be formed as,

$$\cos(\theta 1) + \cos(\theta 2) + \cos(\theta 3) + \cos(\theta 4) = 4ma \quad (6)$$

$$\cos(5\theta 1) + \cos(5\theta 2) + \cos(5\theta 3) + \cos(5\theta 4) = 0 \quad (7)$$

$$\cos(7\theta 1) + \cos(7\theta 2) + \cos(7\theta 3) + \cos(7\theta 4) = 0 \quad (8)$$

$$\cos(9\theta 1) + \cos(9\theta 2) + \cos(9\theta 3) + \cos(9\theta 4) = 0 \quad (9)$$

MI	Switching Angles in Radians			
	Θ_1	Θ_2	Θ_3	Θ_4
0.75	0.1307	0.2652	0.6227	1.5708
0.8	0.1718	0.3558	0.6704	1.0546
0.85	0.0677	0.3676	0.4693	0.9466
0.9	0.0394	0.2395	0.3960	0.6849

Table 1. Switching Angles

1.2 MATLAB SIMULATION STUDY

The trinary 9-level inverter is modelled with the help of MATLAB/SIMULINK software. Two input voltage sources are used i.e 80.25V & 240.75V. All switches here are considered to be ideal. To give desired firing angles to all switches, pulse generator is used. Simulation figure is shown in figure 3

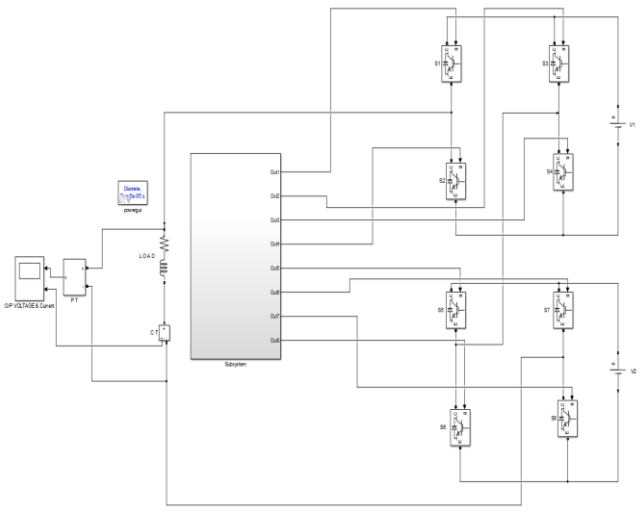

Fig 3 : Simulink diagram of trinary 9-level inverter

Switching pulses are given as per the firing angles calculated are shown in fig 4.

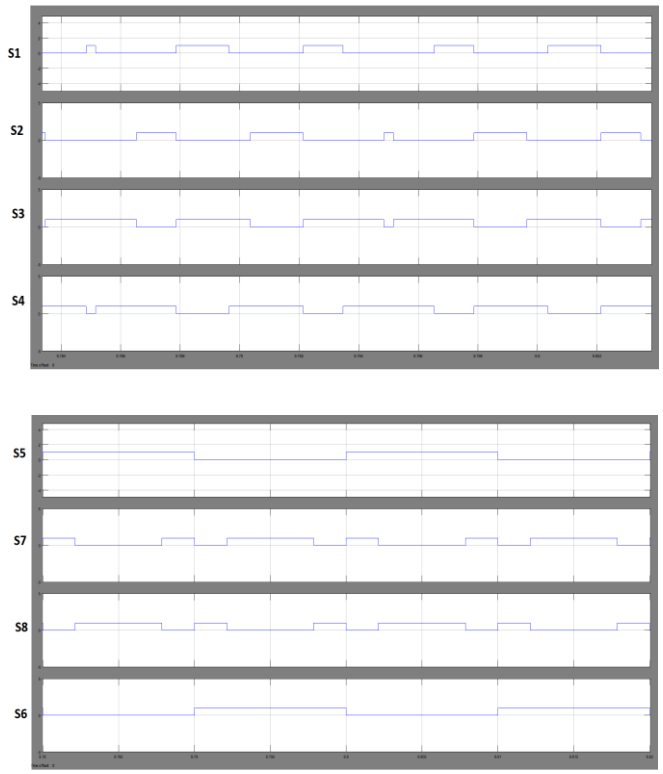

Fig 4: Switching signals for the switches

2. BLOCK DIAGRAM

Single phase trinary asymmetric cascaded H-bridge nine level inverter is implemented in real time.. The various units involved in the fabrication of hardware are power supply unit, rectifier unit, ARDUINO UNO controller, gate driver circuit and multilevel inverter. Driver circuits operate at t voltage levels, hence multi-output power supply unit becomes a vital part of the proposed system. The controller used in the proposed system is ARDUINO UNO controller which operates at +5V DC supply. To implement the hardware of the proposed inverter, MOSFETs IRF840 can be used as switches. TLP250 Gate Driver circuit is used For giving gate pulses.

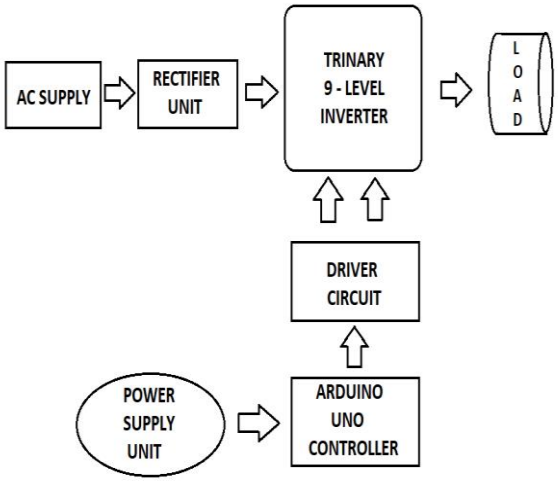

Fig V : Block diagram of experimental setup

Rectifier unit consists of two rectifiers which are used to supply bridge-1 and bridge-2 of the asymmetric cascaded inverter. Single phase AC supply of 90V and 270V is given to rectifier unit to get DC voltages of 80V and 240V respectively. The main advantage of this controller is the ability to generate PWM pulses in real time using control algorithm. This reduces the computational time which required to determine the switching times for inverter legs and makes the system more suitable in case of real time implementation for larger drives.

3. CONCLUSIONS

In this project, a detailed analysis of trinary cascaded H-bridge multilevel inverter topology is presented. GA optimization method is applied to trinary cascaded multilevel inverters. Topology presented in this chapter use less number of switches compared to the symmetric cascaded H-bridge inverter. Comparing the simulation results, trinary asymmetric cascaded nine level inverter shows better performance and also uses the same number of switches used in the binary asymmetric cascaded seven level inverter.

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