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Comparative Analysis and Designing of High Performance and Low Power XNOR Gate Circuit using Hybrid Sleep-Stack (MTCMOS) Technique

Mr. Kamlesh Kumar[1], Mr. Mohit Dahiya[2], Mr. Manoj Kumar[3], Mr. Priyanshu Lakra[4]

[1]Scientist 'D', Ministry of Electronics and Information Technology (MeitY), Government of India
[2]Project Engineer, CDAC-T, posted at Ministry of Electronics and Information Technology (MeitY)
[3] Project Assistant, IIT Hyderabad, posted at Ministry of Electronics and Information Technology (MeitY)
[4]Project Engineer, CDAC-Hyderabad, posted at Ministry of Electronics and Information Technology (MeitY)

Abstract - *The power usage had a significant role in integrated circuits and also enumerated as one of the topmost 3 challenges in the world semiconductor devices technology map. The low-powered club has become a significant factor in recent changes to VLSI. This paper presents examples of pre-designing a low-level 2T XNOR unit at low voltages and consume less amount of power that existing design in this paper newly designed XNOR unit is compared with other low power XNOR units. The core determination of new strategy is to reduce usage of power and reduce absolute voltage to achieve low power as well as voltage of supply. In that article, 2T XNOR gate through MTCMOS. This MTCMOS technology without comparison is compared by considering power as a measurement according to different temperature, frequency and voltage. The designed circuits are tested on 32nm technology of XNOR design with MTCMOS technology for minimum usage of power.*

Key Words: **Low Power, MTCMOS, XNOR, High Performance, CMOS**

1.INTRODUCTION

In huge scope joining (VLSI) plan expansion in semiconductor thickness, power utilization and scaling of size of CMOS become a vital imperative. The scattering of power of circuit that designed using CMOS incorporates dynamic as well as static force dissemination. At the point when structure is present in dynamic operation, power in dynamic mode stays in the circuit. Acc. to design of CMOS circuit the exchanging and power of short circuit is determined. Discharging and charging of the capacitive load that bases power switching as well as charging of interior hub prompts impede scattering. The gate encouraged leakage of subthreshold, drain and gate leakage and oxide tunneling are the fore most factor of dissipation of power leakage [1]. The current leakage increments as gadget sizing or scaling happens that leads to expands the all-out power dissemination of CMOS circuit [2].

The power supply can be decreased by increasing the voltage supply. The supply of DC current along a dimensional scale began with the half-micrometer technology but the size of the electric field causes effect on the speediness of circuit, so the required time for performing execution reduces [5-6]. Attempts to design high speed and low power circuits using MTCMOS that leads to high-speed execution of circuits, emerging as a promising option for building high-speed logic gates that consumes less power than previous existing CMOS structure design. MTCMOS is an efficient step-by-step technology delivers low power and high-performance design uses high and voltage transistors as well as this strategy that practices to reduce low flow of emergency mode while maintaining circuit performance [4].

The lifetime of battery of a cell phone can controlled by reducing or stopping their spillage during rest mode. Abundant static methodologies have developed to decrease the current in static form in circuit of CMOS design [3]. The Power gating methods are generally utilized in late situation, where power in static form being able to decreased by PMOS header or NMOS footer with high value of voltage at threshold level. Through turning off or on of power switches, allow measure of the exchanging energy able to brought down through utilizing the innovative power gating along the charge reusing procedure. At both in sleeping as well as in working mode, the sharing of charge of exchanging of energy occurs in between a virtual VSS & effective VDD lines. Here, effective VSS and VDD connection are attached to power and ground through the NMOS and PMOS individually.

The charge reused plan is able drop extra energy as in comparison with mode of rest than conservative force gating methods deprived of utilizing sharing of charge scheme. In adjusting virtual VSS and VDD lines, the charge reused method of power gating wants extra time and thusly awaken time is extensive. Rest mode of fine grain leakage is supplementary than the coarse grain leakage. As compared to conventional power gating techniques dual power technique is fast [5]. Various factors should be considered before successful implementation of the circuit which includes leakage of power-gate, switching capacitance, size and slew rate of power-gate.

Nowadays, high speed low power CMOS design is the most stimulating concerns in VLSI technology. As the VLSI technology is increasing towards the scaling reduction of technology, the consumption of static power had twisted into a remarkable concern. This research work term paper incorporates the comparison following gating technique of power reduction such as leakage control transistor technique (LECTOR), stack & sleep strategy, sleepy-stack strategy, sleepy keeper strategy, and sleepy keeper leakage control transistor strategy (SK-LCT) for reduction of leakage of power [7]. In this paper, XNOR gate is designed with MTCMOS-Power gating structure technique considering consumption of power as a parameter by changing frequency, temperature and voltage. The designs are verified with 32nm devices library files. A 2T XNOR gate design with MTCMOS technique results out minimum power consumption All the circuit designing and executions had been implemented with 32 nm library files on EDA Tool version 12.6.

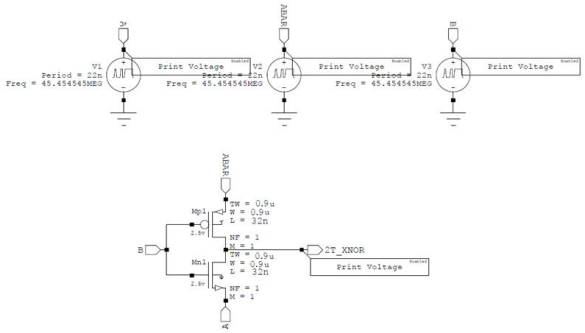

FIG 1: - Schematic of 2T XNOR gate designed in S-Edit of EDA Tool

The power gating method is utilized to minimize dissipation of static power of integrated CMOS circuit by switching the power supply of the circuit for short interval of time. The power gating technique is also used in the testing of the CMOS circuit. The general working of the power gating method is externally switching of the power supply and reduce the power leakage. In mostly CMOS circuit during the standby mode, leakage power is main cause of reduction in the efficiency of the circuit. The majorly used power gating techniques which are used in the CMOS circuits are sleep technique, stack technique, sleepy stack technique which are also called MTCMOS power gating structure techniques.

2. Hybrid sleep-stack (MTCMOS) technique

There is effect on the leakage current at sub-threshold point as the geometry of device scales down. Backup leakage current will turn out to be equal to the dynamic power dissipation in various different circumstances, which is due to power supply and threshold voltage scaling. To increase battery life of the mobile devices, leakage current at standby mode that could reduced which is due to high standby period [8]. MTCMOS is one of the utmost operative technique to diminish the power leakage of the circuit. In MTCMOS technique, there are two different modes of operation, standby mode & active mode. It consists of two threshold transistors where as in general there is only single threshold transistor (V_t) in the CMOS circuit. There are two types of transistors used in the MTCMOS technique, one is high threshold voltage transistor (i.e., high V_t)) called sleep transistor, which is used in averting dissipation of leakage power and other is low threshold voltage transistor (i.e., low V_t) which is used to enhance the performance of circuit. One of the sleep transistor that is placed in between the pull-up network and power supply and other is placed between pull down and ground. Two complementary signals are applied to these networks [1].

The S Edit circuit shown below, operates in active and standby mode. In active mode, while TBAR is HIGH and T is LOW then both the snooze transistors are turned ON, in this condition it works as normal CMOS circuit. During operation at standby mode, T is HIGH and TBAR is LOW then it turns off the sleep transistors, resulting in high resistance from VDD to Ground that will reduce the leakage power.

3. Design of XNOR gate using Hybrid sleep-stack (MTCMOS) technique

The designed circuit of XNOR gate as shown in figure, contains two transistors one PMOS, PM1 and one NMOS, NM1. Operation of the XNOR gate is dependent on the inputs A and B. When both the input is low (A=0, B=0) then NMOS is switched OFF and PMOS is switched ON due to large voltage of gate then threshold. And PMOS in this case pass high output (Out=1) logic.

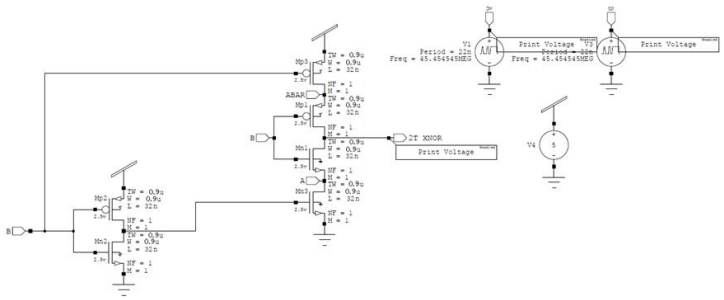

FIG 2: - Schematic of 2T XNOR gate of Hybrid sleep-stack (MTCMOS) technique in S-Edit of EDA Tool

When one of the inputs is high (A=0, B=1) or (A=1, B=0), in this case the NMOS is ON but overall output is low (Out=0) ignoring the effect of PMOS being ON. When both the inputs are high (A=1, B=1) then the NMOS transistors are ON which will drive the high output signal and PMOS is OFF.

4. RESULTS

All the schematic simulations are executed on EDA tool at 32 nm technology at diverse input voltage level that ranges in between 0.3 to 0.9V in small intervals of 0.1V. Both the XNOR circuits will be tested with same input patterns. The 2T XNOR gate with MTCMOS is observed that it shows enhanced performance than the pre-existing XNOR gate.

Table -1: Presentation Table of 2T XNOR gate

A (Input)	B (Input)	Estimated Outcome	Attained output
0	1	1	0.001
1	1	0	1.001
0	0	0	1.001
1	0	1	0.001

4.1 Simulation of the circuit results in EDA tool

It is observed that using various above-mentioned technique has enhanced temperature sustainability and suggestively power delay product (PDP) & less power at numerous different input frequencies & voltages.

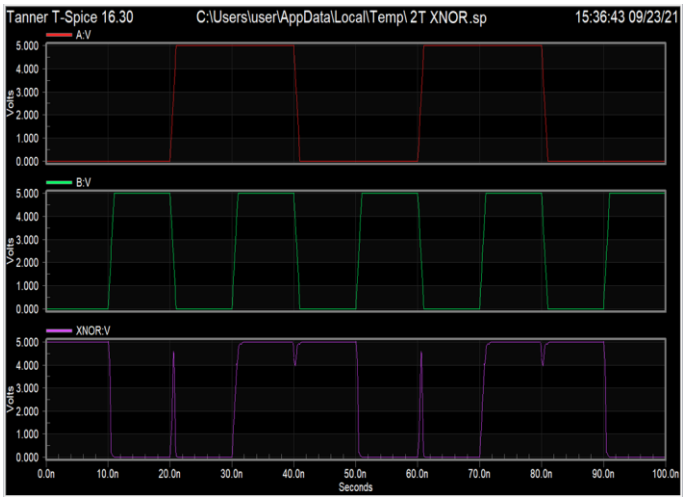

FIG 3: Output 2T XNOR gate of Hybrid sleep-stack (MTCMOS) technique in S-Edit of EDA Tool

MTCMOS designed circuitry have a drawback that it causes minimal escalation of area as associated to the CMOS circuit. Generally, we realized the dissipation of minimal power through MTCMOS technique.

Table -2: Power Delay Product Vs Voltage Analysis

VOLTAGE (V)	POWER DELAY PRODUCT		
	EXISTING CIRCUIT	MTCMOS 3T XNOR	MTCMOS 2T XNOR
0.5	6E-13	3E-13	1E-13
0.6	9E-13	4E-13	2E-13
0.7	1.3E-12	9E-13	5E-13
0.8	1.4E-12	1.1E-12	6E-13
0.9	1.7E-12	1.3E-12	9E-13

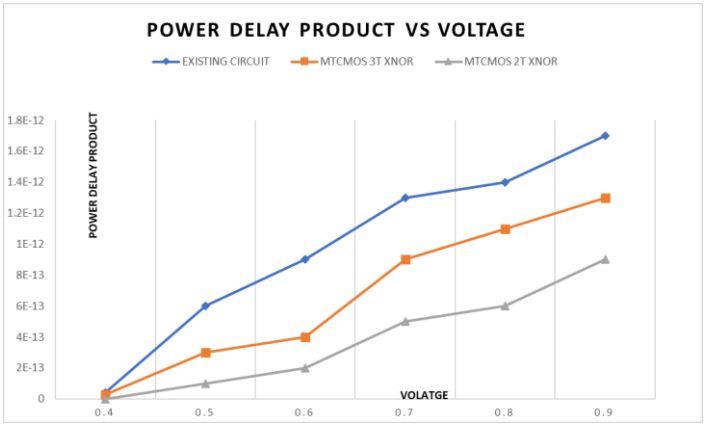

Chart -1: PDP Vs Voltage of existing circuit, MTCMOS 3T XNOR and MTCMOS 2T XNOR

Table -3: Power Consumption Vs Voltage Analysis

VOLTAGE (V)	POWER CONSUMPTION (Watt)		
	EXISTING CIRCUIT	MTCMOS 3T XNOR	MTCMOS 2T XNOR
0.4	0.00004	0.00003	0.00001
0.5	0.00007	0.00003	0.00002
0.6	0.00012	0.00009	0.00007
0.7	0.00015	0.000116	0.000101
0.8	0.00022	0.00019	0.00017

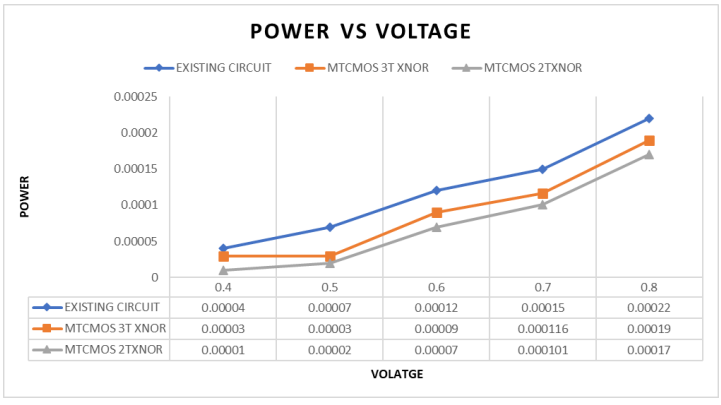

Chart -2: Power Vs Voltage of existing circuit, MTCMOS 3T XNOR and MTCMOS 2T XNOR

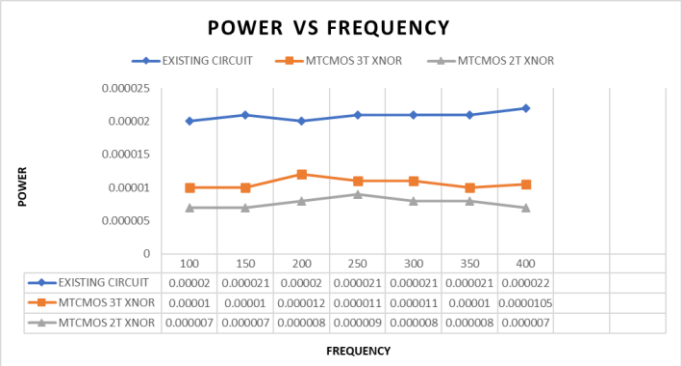

Chart -3: Power Vs Frequency of existing circuit, MTCMOS 3T XNOR and MTCMOS 2T XNOR

5. CONCLUSION

The 2T XNOR gate is designed, simulated and compared with existing XNOR units and simulated on the Tanner EDA version 16.3 instrument on 32 nm technology. The 2T XNOR gate with MTCMOS is said to give better performance than the existing XNOR gate. It is tested for superior temperature stability and provides significantly lower power and power latency at various input voltages and frequencies. MTCMOS circuits have a slightly increased area compared to CMOS circuits; Overall, we achieved the lowest power consumption with MTCMOS technology.

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BIOGRAPHIES

Mr. Kamlesh Kumar received B.Tech degree in Electronics & Communication Engineering (ECE) from Maharaja Agrasen Institute of Technology, G.G.S.I.P. University, New Delhi, India in 2010. He is currently working as Scientist 'D' in Ministry of Electronics and Information Technology (MeitY), Government of India and involve in various R&D activity in the Ministry. Before Joining MeitY, he served in India Meteorological Department (IMD) under Ministry of Earth Science as Scientific Assistant and work on Different weather forecasting activity including Radar, Synop, Aviation Meteorology also he served in HCL Technology as Software Engineer for two years and worked on different tools, i.e., Load Runner, QTP, Selenium. His research area is Converged Communication, Strategic / Industrial Electronics including IoT and Cognitive Radio and Intelligent Transportation System (ITS).

Mr. Mohit Dahiya, received B.Tech in Electronics and Communication Engineering from Maharaja Surajmal Institute of Technology, affiliated by Guru Gobind Singh University in year of 2019 and currently pursuing M.Tech in Electronics and Communication from University School of Information Communication and Technology (GGSIPU). He is currently working as Project Engineer in Centre Development of Advance Computing (C-DAC), posted at

Ministry of Electronics and Information Technology (MeitY) on projects of Intelligent Transportation System (InTranSE). His core skills include RTL Coding using Synthesizable constructs of Verilog | Simulation | CMOS Fundamentals Code Coverage |Functional Coverage | Synthesis. VLSI Domain Skills in HDL-Verilog | HVL-System Verilog | Verification Methodologies- Constraint Random Coverage Driven Verification, Assertion Based Verification- SVA | TB Methodology- UVM.

Mr. Manoj Kumar, received B.Tech in Electrical and Electronics Engineering from Northern India Engineering college , affiliated to Guru Gobind Singh Indraprastha University in the year of 2018 and currently pursuing M.Tech in Electronics and Communication Engineering from University school of Information and Communication Technology (GGSIPU).He has worked on low power application devices and published the research on the same and He is currently working as Project Assistant in IIT Hyderabad, posted at Ministry of Electronics and Information Technology (MeitY) on project "Real Time Edge Computing Architectures for LiDAR based Intelligent Transportation System". His core skills include PCB Designing | Motor and Drives | PLC & SCADA | Mentor Graphics EDA Tool.

Mr. Priyanshu Lakra, completed his B.Tech in Electronics and Communication Engineering from Ansal University, Gurgaon in the year of 2018 and currently pursuing M.Tech in Electronics and Communication Engineering from University School of Information and Communication Technology (USICT) of Guru Gobind Singh Indraprastha University (GGSIPU). He is currently working as Project Engineer in Centre Development of Advance Computing (C-DAC), posted at Ministry of Electronics and Information Technology (MeitY) His core skills are Mentor Graphics EDA Tool |VLSI | PCB Designing | Digital electronics. VLSI Domain Skills in HDL-Verilog | HVL-System Verilog | Verification Methodologies- Constraint Random Coverage Driven Verification.