International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 09 Issue: 06 | June 2022 www.irjet.net p-ISSN: 2395-0072

Design and Performance Analysis of 8 x 8 Network on Chip Router

Preethi T S[1], Jayanth K Holalkeri[2], Manasa Dev G J[3], Manoj M Biradar[4], Nagesh R Shanbhag[5]

[1]*Assistant Professor, Dept. of Electronics and Communication Engineering, Sapthagiri College of Engineering, Karnataka, India*

[2345] *Student, Dept. of Electronics and Communication Engineering, Sapthagiri College of Engineering, Karnataka, India*

Abstract – *Network on chip is a new prototype model in complex system-on-chips that provide an effective on chip communication networks. The information is transmitted through the interconnected modules in terms of packets. The main task of router is routing the data. So, the router architecture must be efficient with lower latency and higher throughput. In this project, we design and implement a 2D Network-on-Chip router mesh having four ports connected to other ports in four directions, namely North, South, West, East, and the fifth connected to the Local processing element through a network interface. This project is aimed to improve "Quality-of-Service" by employing algorithms like wormhole, routing, arbiter and crossbar switching.*

Key Words: **Bandwidth reservation, Flitting, Label switching, Networks-on-chip, Quality of Service, Streaming applications, System-on-Chip.**

1. INTRODUCTION

The recent technological advancements in the domain of semiconductor integration technology is to fill the number of working transistors on an available chip area for fabrication, satisfying the Moore's law as shown in Fig-1, which resulted in developments of techniques and technologies in the field of System on Chip, hence this has resulted with new arena to the work space of miniaturization and this has highly influenced by gate level circuit association for the Application Specific Integrated Circuit (ASIC). Then technologies have to be developed in-line with the demands of market space and design time for execution, all these criteria of innovations to meet the needs of communication in the existing domain which lead the scope for the evolving of networking on the same silicon chip for communicates leading to the era of Network on Chip.

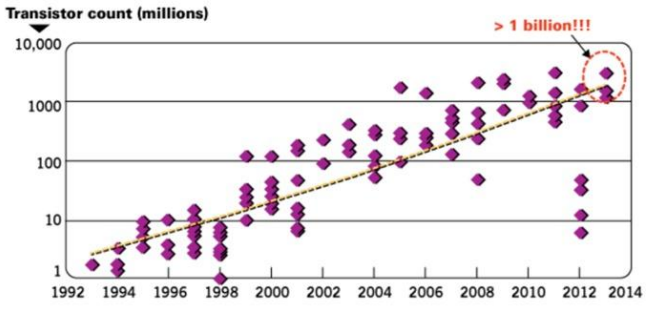

Fig -1: Evolution of transistor integration on a chip

Network on-chip is one such innovation known for its adaptation and flexibility of operation over the chip by satisfying the factor of power, area and number of gates. The ASIC and SoC design approaches are well suited for various integration of peripherals with its approaches meeting the architectural requirement for the minimization of the delay and effective communication among the devices in both simplex and duplex communication criteria. This leads to the simplification of various redundant interconnections among various peripherals in the connection platform which should be fault tolerant as well for successive implementation of the desired system. But in the present scenario, for the effective on-chip communication design, SoC is the best suited option but not fair enough for the effective communication among the peripherals. Hence, it requires reframing of the architecture to achieve minimum delay with maximum reliability, which can be obtained by interfacing NoC with SoC.

NoC based systems also play a vital role for data exchange. To meet the needs and requirements of data handling over the different types of topology and algorithms for memory or buffer-based data transmission on an FPGA device, it requires Dynamically Reconfigurable NoC (DRNOC). In this project we are bound to design a router under two-dimensional structure. Later the design is proposed in generalizing to N x N structure for the improvement of the properties of the FPGA viz, delay, throughput, LUT and flip□flops using Xilinx ISE platform for simulation and testing of the properties comparatively over the existing systems.

2. LITERATURE SURVEY

The paper [1] proposes switch model design and implementation for students' laboratory activities. The three staged switching architecture comprising of software and hardware systems which are based on modular 3x3 switches, with controller as an Arduino microcontroller. The switch uses a few stages of smaller NxN crossbar switches to help in producing non-blocking connections and forming an NxN network. As the tiniest component within which a switching system exists, is a squared cross-bar switch. This switch has to be designed in such a way that it should be able to connect all inputs to all its outputs. The blocking is due to busy destination as the experiment conducted also it showcases 94% successful connections while 6% blocking is not caused due to busy switches, but due to busy destinations.

The paper [6] examines the impact of failures on the reliability of the chips and develops corelating passive counter protocols either to prevent or recover from them. In this view, several schemes were adapted in order to reduce various kinds of error symptoms, while area and power are at a minimum. Over a normal transmission scheme, it requires a 3-flitting re-transmission buffer per virtual, since a flit must be kept for 3 cycles after it leaves the current node. The least complex type of transmission buffer is a Queue working on the principle of First-In First-Out (FIFO) buffer [25]. Such implementation type has one input port and one output port, and has a control logic. The concept of deadlock has been enormously stressed upon. Some of errors mainly encountered in the router are VC allocator error, crossbar error, handshaking error. The scheme turned out to be highly effective both in terms of latency and power even under high error rates. All of these mechanisms described in the work helps in keeping the critical path of the Network on Chip router intact.

The work proposed in [9] describes the design of on chip routers based on power consumed and its area occupied by chip. Proposed architecture of on-chip router in this gives the results in which power consumption is reduced and silicon area is also minimized. This router for NoC increases throughput, and introduces architecture which shows an improvement in Figure of Merit. But increases the area and power due to extra crossbar and arbiter scheme, and got up to 94% of throughput, while power consumption is increased by the factor of 1.28. [10] This approach reduces power consumption. It also points at the buffer utilization by making the channels bidirectional and shows drastic improvement in the performance of system. A router architecture with Reliability Aware Virtual Router allocates more memory to the busy channels and less to the idle channels. This solution is delay efficient but not area and power efficient.

The paper [20] presents how a NoC topology, routing algorithm and switching are vital in communication. In any NoC architecture, routing algorithm is an important key factor. The path chosen by the packet from source to destination is defined by a routing algorithm. XY algorithm is one of the simplest routing algorithms used in NOC. The paper reviews a different XY routing algorithm that is implemented. The use of this algorithm is totally dependent on the application and environment. The selection of which totally depends on the application and the traffic of packets in the network. Because the simplicity in implementation is important in all architecture, XY routing algorithm is widely used. The Dynamic-XY routing algorithm achieves better balance in load distribution and also provides deadlock-free and livelock-free facility where the user can't compromise with accuracy of data received, they go for the fault-tolerant routing like XYX. Finally, we can conclude that the choice of XY routing algorithm is totally dependent upon environmental condition of NOC architecture.

The paper [14] proposed an approach to find the shortest path distance between two nodes implementing on FPGA technology. The FPGA articulates parallelism to significantly reduce steps as compared to sequential effort. In this paper, A* algorithm is chosen for the shortest path distance calculation based on its heuristic behavior since it achieves superior time running. Shortest path algorithms are applied for applications like transportation and networking. If the shortest path is calculated on general purpose processor, to read the input there are separate instructions, and then compute the result to produce the output which slows down the overall performance. The research work reduces delay in finding the shortest path. This research [14] contributes in finding the shortest path with reduced delay by taking advantage of parallel processing in FPGA. A new design in coprocessor implementation is proposed using A* algorithms technique, and using this brings in the concept of parallelism.

3. SCOPE OF WORK

Based on the literature survey and various studies, in this paper we are bound to design a Label Switching Network on Chip router comprising of following:

1. Crossbar switch to establish a connection from each input to each output.
2. Arbiter module to check port validity and to flit.
3. A NoC manager used for bandwidth allocation.
4. A LS router that checks if the router is valid or not.

We design and implement all the modules mentioned above, using Xilinx ISE 14.7 and instantiate it in a top module to form a single router. Further we implement power optimization techniques to reduce the power and improve QoS.

4. METHODOLOGY

The following steps are carried out to form an 8x8 NoC Router.

4.1 To Design a Crossbar Switch

A Crossbar switch is designed in Xilinx ISE as shown in Fig-2.

1. Every on chip router has 5 ports namely, Local, East, West, North and South.
2. Every port needs to have one multiplexer, therefore for five ports we need five MUX.
3. The crossbar module has seven input ports and five output ports and five wires for intermediate connections.

4. The 5bit enable bus is used to enable the particular MUX and 3bit select line is used to connect input to a particular output.

5. Every possible condition of enable and select lines are specified and based on that condition the incoming ports and output ports are connected.

6. The select line bits are determined by the arbiter module discussed below.

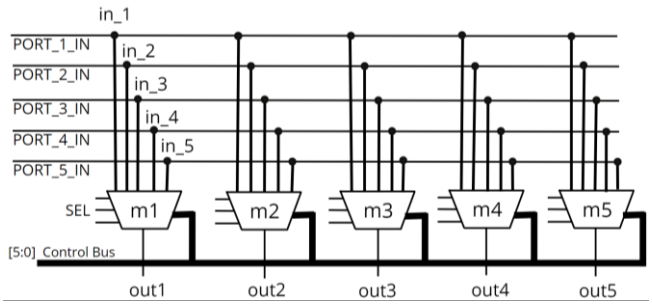

Fig -2: Crossbar Switch using MUX

4.2 To Design an Arbiter module

An arbiter module is designed in Xilinx ISE and the RTL schematic is shown in Fig-3.

1. An arbiter module is designed using arbiter algorithm and it consists of 5 input ports and 6 output ports.

2. This module helps to flit the message bits.

3. Based on the condition of the destination ID and label, it checks the validity of the port.

4. Inferring the select conditions of all the five ports, the output port is allocated with the select line bits used in crossbar module.

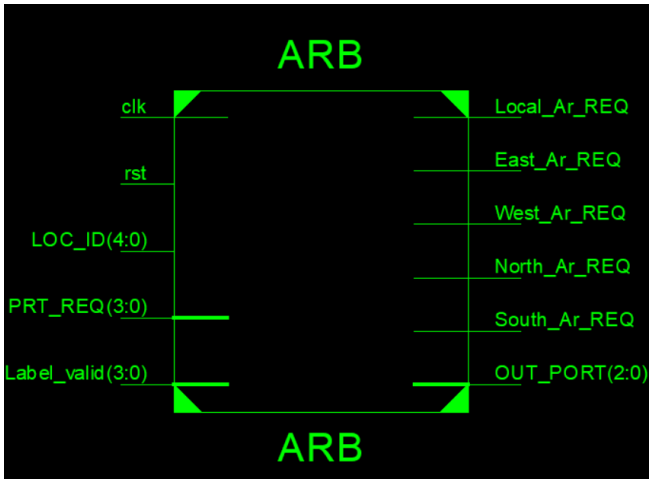

Fig -3: RTL Schematic of Arbiter module

4.3 To Design an NoC Manager

An NoC manager is designed and the RTL schematic is shown in Fig-4.

1. NoC manager is used to monitor the used and the unused bandwidth.

2. It mainly works on the principle of edge detection.

3. Edge detection between two corresponding routers is done by considering LSB bits as shown in Fig-5.

4. Every port has one NoC manager, so for five ports there are five NoC manager present in a single router.

5. Scaling factor is set to 5 between two slots and 2 between the packets in one slot.

6. Only if the bandwidth is greater than 2, the port is considered to be available.

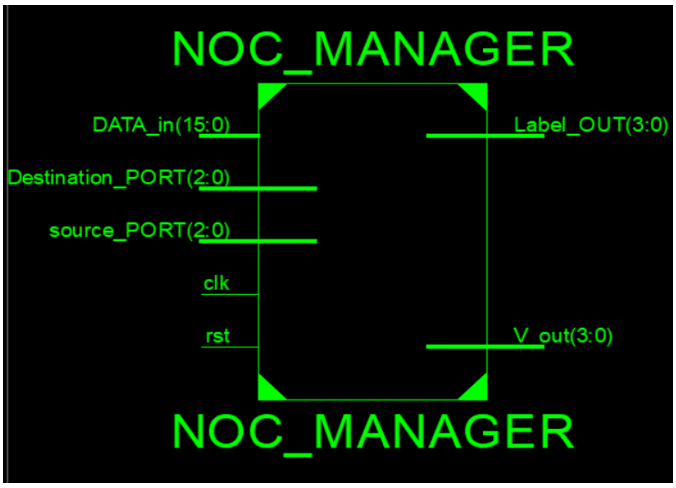

Fig -4: RTL Schematic of NoC manager

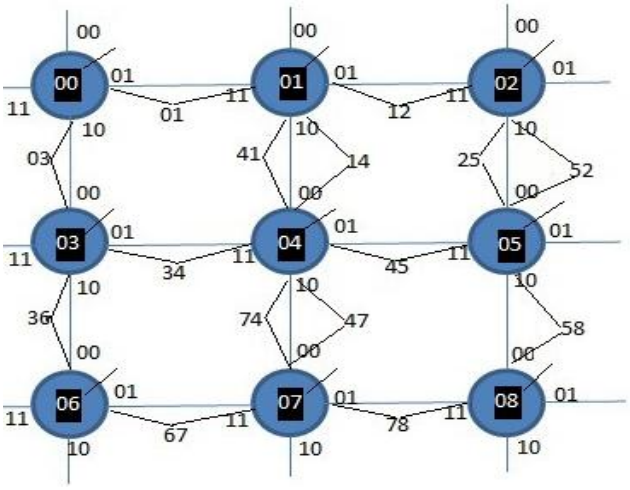

Fig -5: Edge Detection occurring in NoC manager

4.4 To Design a Label Switched Router

Label switched router is designed and the RTL schematic is shown in Fig-6.

1. A label-based switching router is connected to all the five ports.
2. It also consists of a Queue module which implements FIFO operation.
3. It is used to generate labels and to check whether port is valid or not.
4. It checks whether received packet is valid or not and whether the packet is successfully transmitted or not.
5. It also checks congestion of the port, if the port is in use the packet is buffered in FIFO module and whether the FIFO is full or not.

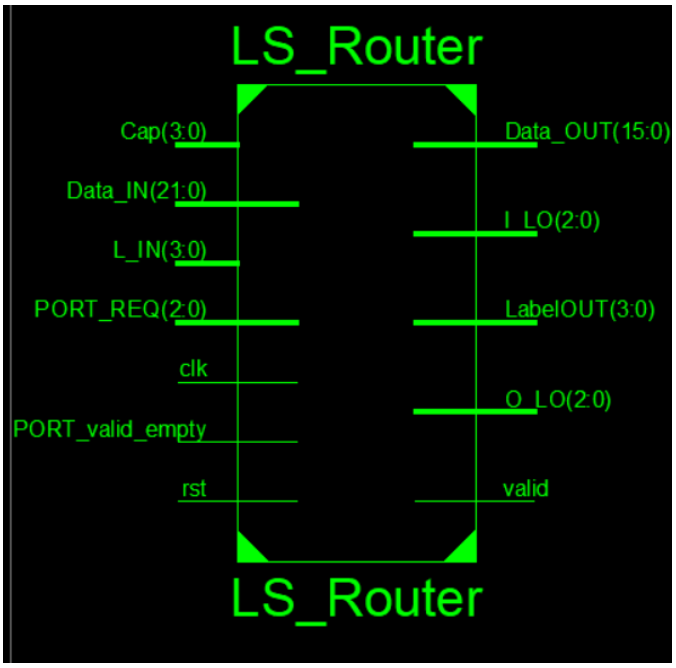

Fig -6: RTL Schematic of LS Router

5. RESULTS OF THE PROJECT

5.1 Simulation of the project.

Crossbar Switch and Arbiter module are simulated and verified its operation successfully. The simulation results of crossbar and arbiter module are shown in Fig-7 and Fig-8 respectively.

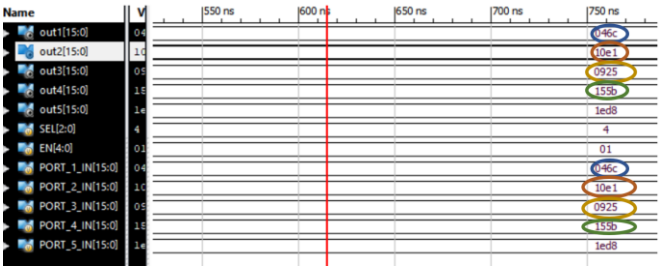

Fig -7: Simulation results of Crossbar module

Fig -8: Simulation results of Arbiter module

The specifications for this project is mentioned in Table-1.

Table -1: Design Specification

Sl.	Specification	Value
1.	Design Topology	2D Mesh
2.	Size	8x8
3.	Switching Mechanism	Crossbar
4.	Packet Format	Header, Message
5.	Routing Algorithm	Deterministic XY
6.	Packet Size	22 bits
7.	Simulation Tool	Xilinx ISE 14.7
8.	Kit	FPGA Spartan 6

Once all the sub-blocks are designed and verified, we instantiate all the modules in the top module to form a single router. A packet format of 22 bits is considered of which 6 bits denote the source and destination address, remaining 16 bits denotes the message. Then the single router is multiplied 9 times to form a 3x3 router, and 64 times to form a 8x8 router. To verify the functionality of 8x8 router, initially a test bench is written and simulated. The simulation results of the 8x8 router are shown in Fig-9.

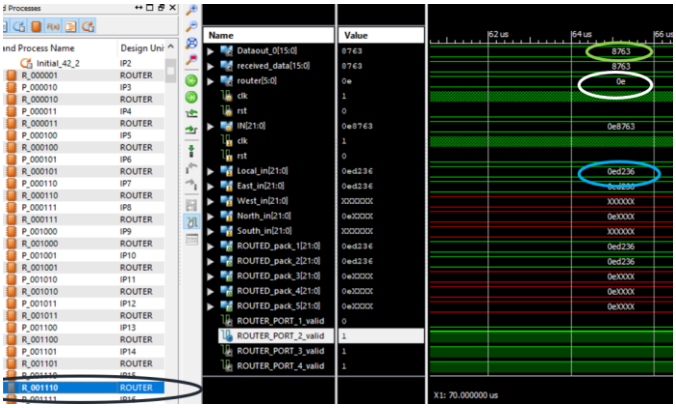

Fig -9: Simulation results of 8 x 8 router

5.2 Power and Area Optimization

Before implementing it on the FPGA, we have written an algorithm to optimize the power. The algorithm is aimed to reduce the transitions in the message bits. For this we adopted the encoding and decoding techniques. Before transmitting the message is encoded using the bits b1 and b2. Any combination of b1 and b2 can be taken, but in this project, we have taken b1 as 0 and b2 as 1. All the even bits are XOR with b1 and odd bits are XOR with b1 and b2. The same decoding technique is used at the receiver to retrieve the original message. An example is shown in Fig-10. From the figure we can see that the number of transitions is reduced from 6 to 3, which reduces the power consumption during the process of transmitting.

Let x=1110010101 Number of transitions: 6
b1=0
b2=1
z[0] = x[0] ^ b1 = 1 ^ 0 = 1
z[1] = x[1] ^ b1 ^ b2 = 0 ^ 0 ^ 1 = 1
z[2] = x[2] ^ b1 = 1 ^ 0 = 1
z[3] = x[3] ^ b1 ^ b2 = 0 ^ 0 ^ 1 = 1
z[4] = x[4] ^ b1 = 1 ^ 0 = 1
z[5] = x[5] ^ b1 ^ b2 = 0 ^ 0 ^ 1 = 1
z[6] = x[6] ^ b1 = 0 ^ 0 = 0
z[7] = x[7] ^ b1 ^ b2 = 1 ^ 0 ^ 1 = 1
z[8] = x[8] ^ b1 = 1 ^ 0 = 1
z[9] = x[9] ^ b1 ^ b2 = 1 ^ 0 ^ 1 = 0
Encoded sequence: 1111110010 Number of transitions: 3

Fig -10: Power Optimization Technique

After successful verification of 8x8 router, it is implemented on FPGA Spartan 6. The power consumption is observed to be 0.085W as shown in Fig-11. The area details in the design summary are shown in Table -2.

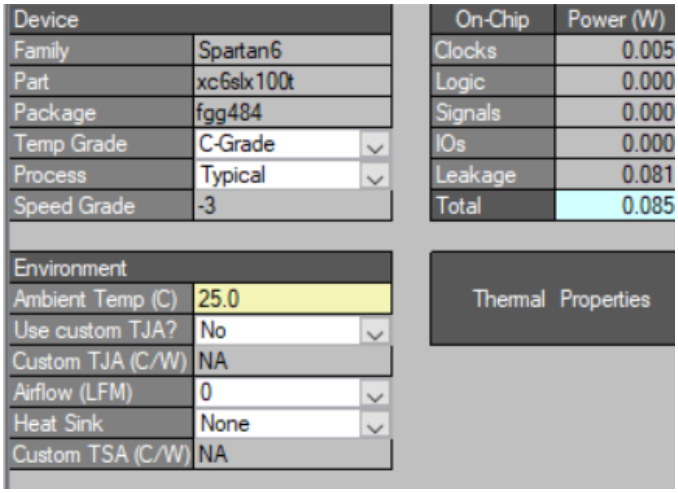

Fig -11: Power Consumption Report

Table -2: Design Summary

Logic Utilization	Used	Available	Utilization
No. of Slice registers	21,325	126,576	16%
No. of Slice LUTs	28,005	63,288	44%
No. of occupied Slices	9,974	15,822	63%
No. of IOBs	40	296	13%

ChipScope Tool is used to implement the project and additional files required to implement are written and added as a source to the top module. Data port width is taken as 57 and classified 16 ports for sending data, 16 ports for receiving data, 16 bits for the data, 4 bits for expected and arrived port and 1 port for reset. Then trigger setup is done and waveform is added to the window. The implementation and its results are shown in Fig-1.

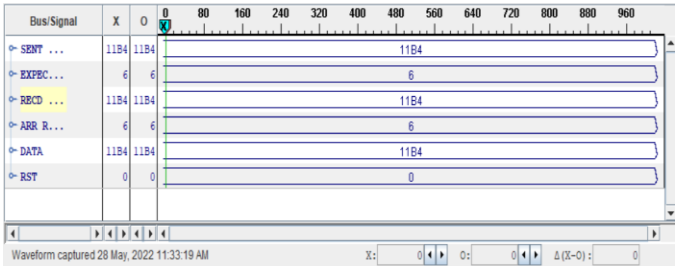

Fig -13: Implementation results using ChipScope

6. CONCLUSION

The various challenges in SoC design made the researchers look for better alternatives that made a way for Network on chip technology. The NoC is currently still in its initial stages and emerging research area. NoC has a remarkable impact on the SoC design of next generation and multicore architectures. For this project, various surveys and recent

research aspects of NoC, routing algorithms and network topology details were explored. An attempt was made to contribute in the research of NoC by exploring the space of NoC router design which is a predominant component of the network. The main focus of this project is to design an efficient router since it is one of the most important components that determines various network parameters like latency, throughput and delay. The designing and simulation have been done using the hardware description language Verilog HDL in Xilinx ISE tool and implemented on Field Programmable Gate Array, using ChipScope Tool.

REFERENCES

[1] Sani. A. and Fauzi. R, "Crossbar switch module implementation for laboratory purpose", In Journal of Physics: Conference Series, Vol. 1235, No. 1, p. 012042, IOP Publishing, June 2019.

[2] Islam, M.A., Arafath, M.Y. and Hasan, M.J., "Design of DDR4 SDRAM controller", In 8th International Conference on Electrical and Computer Engineering, IEEE, pp 148- 151, December 2014.

[3] Nikologiannis, A., Papaefstathiou, I., Kornaros, G. and Kachris, C., "An FPGA-based queue management system for high speed networking devices", Microprocessors and Microsystems, 28(5-6), pp.223-236, 2004.

[4] Agarwal, A., Iskander, C. and Shankar, R., "Survey of network on chip (noc) architectures & contributions", Journal of engineering, Computing and Architecture, 3(1), pp.21-27, 2009.

[5] Hecht, R., Kubisch, S., Herrholtz, A. and Timmermann, D, "Dynamic Reconfiguration with hardwired Networks-on-Chip on future FPGA", In International Conference on Field Programmable Logic and Applications, 2005, IEEE, pp 527-530, August 2005.

[6] Park, D., Nicopoulos, C., Kim, J., Vijaykrishnan, N. and Das, C.R., "Exploring faulttolerant network-on-chip architectures", In International Conference on Dependable Systems and Networks (DSN'06), IEEE, pp 93-104, June 2006.

[7] Tsai, W.C., Lan, Y.C., Hu, Y.H. and Chen, S.J., "Networks on chips: structure and design methodologies", Journal of Electrical and Computer Engineering, 2012.

[8] Corbetta, S., Rana, V., Santambrogio, M.D. and Sciuto, D., "A light-weight Network-onChip architecture for dynamically reconfigurable systems", In 2008 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, IEEE, pp 49-56, July 2008.

[9] Kim, J., Park, D., Nicopoulos, C., Vijaykrishnan, N. and Das, C.R., "Design and analysis of an NoC architecture from performance, reliability and energy perspective", In 2005 Symposium on Architectures for Networking and Communications Systems (ANCS), IEEE, pp. 173-182, October 2005.

[10] Valinataj, M., Mohammadi, S. and Safari, S., "Fault-aware and reconfigurable routing algorithms for Networks-on-Chip", IETE Journal of Research, 57(3), pp 215-223, 2011.

[11] Shilpa. K. Gowda, "On-Chip Network Design with Dynamic Reconfiguration", International Journal of Scientific & Engineering Research, Volume VI, Issue VII, pp 1326-1329, July 2015.

[12] Paramasivam, K., "Network On-Chip and Its Research Challenges", ICTACT Journal on Microelectronics (1.02), 2015.

[13] Seema Sreekumar, "Network on Chip configuration and associated Algorithms", Journal of Emerging Technologies and Innovative Research (JETIR), Volume VIII, Issue III. (ISSN-2349-5162), March 2021.

[14] Idris, M.Y.I., Bakar, S.A., Tamil, E.M., Razak, Z. and Noor, N.M, "High-speed shortest path co-processor design", IEEE In 2009 Third Asia International Conference on Modelling & Simulation, pp 626-631, May 2009.

[15] Sao, P., Agrawal, R., "A Survey of Router Design Algorithms for NoC Platform and their Performance Analysis", International Journal of Latest Technology in Engineering, Management & Applied Science (IJLTEMS), Volume II, Issue VIII, pp 73- 76, 2013.

[16] Cesário, W.O., Lyonnard, D., Nicolescu, G., Paviot, Y., Yoo, S., Jerraya, A.A., Gauthier, L. and Diaz-Nava, M., "Multiprocessor SoC platforms: a component-based design approach", IEEE Design & Test of Computers, 19(6), pp 52-63, 2002.

[17] Sgroi, M., Sheets, M., Mihal, A., Keutzer, K., Malik, S., Rabaey, J. and SangiovanniVincentelli, A., "Addressing the system-on-a-chip interconnect woes through communication-based design", In Proceedings of the 38th Design Automation Conference (IEEE Cat. No. 01CH37232), pp 667-672, June 2001.

[18] Yoo, Sungjoo, Gabriela Nicolescu, Damien Lyonnard, Amer Baghdadi, and Ahmed A. Jerraya, "A generic wrapper architecture for multi-processor SoC co-simulation and design.", In Proceedings of the ninth international symposium on Hardware/software co-design, pp 195-200, 2001.

[19] Bahn, J.H., Lee, S.E. and Bagherzadeh, N., "On design and analysis of a feasible network-on-chip (noc) architecture", In Fourth International Conference on Information Technology (ITNG'07), IEEE, pp 1033-1038, April 2007.

[20] Chawade, S.D., Gaikwad, M.A. and Patrikar, R.M., "Review of XY routing algorithm for network-on-chip architecture", International Journal of Computer Applications(IJCE), 43(21), pp.975-8887, 2012.

[21] Sayankar, B.B., Agrawal, P. and Dorle, S.S., "Routing Algorithms for NoC Architecture: A Relative Analysis", In 2013 6th International Conference on Emerging Trends in Engineering and Technology, IEEE, pp 105-106, December 2013.

[22] Sani, A, "Multistage switching hardware and software implementations for student experiment purpose", In IOP Conference Series: Materials Science and Engineering, Vol. 309, no. 1, p. 012097, 2018.

[23] Talwar, B. and Amrutur, B, "Traffic engineered NoC for streaming applications", Microprocessors and Microsystems, 37(3), pp 333-344, 2013.

[24] Kendaganna, S.S., Jatti, A. and Uma, B.V., "Design and implementation of secured agent based NoC using shortest path routing algorithm", International Journal of Electrical and Computer Engineering(IJECE), 9(2), p.950, 2019.

[25] Yang, Z.J., Kumar, A. and Ha, Y., "An area-efficient dynamically reconfigurable spatial division multiplexing network-on-chip with static throughput guarantee", In 2010 International Conference on Field-Programmable Technology, IEEE, pp. 389-392, December 2010.

BIOGRAPHIES

Preethi T S,
Assistant Professor, Dept. of ECE
Sapthagiri College of Engineering
Email :
ts.preethi@gmail.com

Jayanth K Holalkeri,
Student, Dept. of ECE
Sapthagiri College of Engineering
Email:
jayanth.holalkeri@gmail.com

Manasa Dev G J,
Student, Dept. of ECE
Sapthagiri College of Engineering
Email:
manasadev30@gmail.com

Manoj Mahadev Biradar,
Student, Dept. of ECE
Sapthagiri College of Engineering
Email:
mmbiradar1906@gmail.com

Nagesh R Shanbhag,
Student, Dept. of ECE
Sapthagiri College of Engineering
Email:
nageshrshanbhag619@gmail.com